KFUPM

Spin Qubits in Semiconductors for Scalable Quantum Computers

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Quantum Center at KFUPM, Saudi Arabia



Outline

- spin qubit overview
- (hole) spin qubits in Ge & Si & Sn: heterostructures, nanowires, FinFETs,...
- scaling via interconnects: magnetic racetrack
- classical reversible computing with spin qubits

Reviews: Kloeffel and DL, Annu. Rev. Condens. Matter Phys. 4, 51 (2013)
Chatterjee et al., Nature Reviews Physics 3, 157 (2021)
Burkard,...,Petta et al., RMP 95, 025003 (2023)
Stano and DL, Nature Reviews Physics (2022)
Fang et al., Mater. Quantum Technol. 3, 012003 (2023) (holes)
McIntyre, Sarkar and DL, New J. Phys. 28, 081203 (2026)

Front-Runners for Quantum Computers

- spin qubits in semiconductors
- superconducting devices
- ions, atoms, photons
- topological quantum computing?
  - 'semi-superconductor hybrids' & TIs

See e.g. *Nanomaterials for Quantum Information Science and Engineering*, Alfieri et al., Advanced Materials, 2109621 (2022)

Front-Runners for Quantum Computers

- spin qubits in semiconductors

'small & fast'
Target: 100M qubits for 'FTQC'

- superconducting devices
- ions, atoms, photons

'big & slow'
Now: 100s of qubits for 'NISQ'

- topological quantum computing?

'semi-superconductor hybrids' & TIs

'exotic'
Majorana ?
Para- or Fibonacci fermions?

See e.g. *Nanomaterials for Quantum Information Science and Engineering*, Alfieri et al., Advanced Materials, 2109621 (2022)

Front-Runners for Quantum Computers

- spin qubits in semiconductors

Intel, HRL/IBM, Leti Grenoble, IMEC, DiraQ, Q-Motion, SiliQon, Quobly, Equal1, Groove, C13, Delft, Riken, UCLA, Sydney, Basel/IBM/ETH, EU Q-Flagship,,...

'small & fast'
Target: 100M qubits for 'FTQC'

- superconducting devices

IBM, Google, Rigetti, USTC, D-Wave,…

- ions, atoms, photons

Quantinuum (3 nines's), IonQ, QuEra, Pasqal, Quandela, Xanadu, Atom Comp., PsiQuantum, Infleqtion, and many start-ups

'big & slow'
Now: 100s of qubits for 'NISQ'

- topological quantum computing?

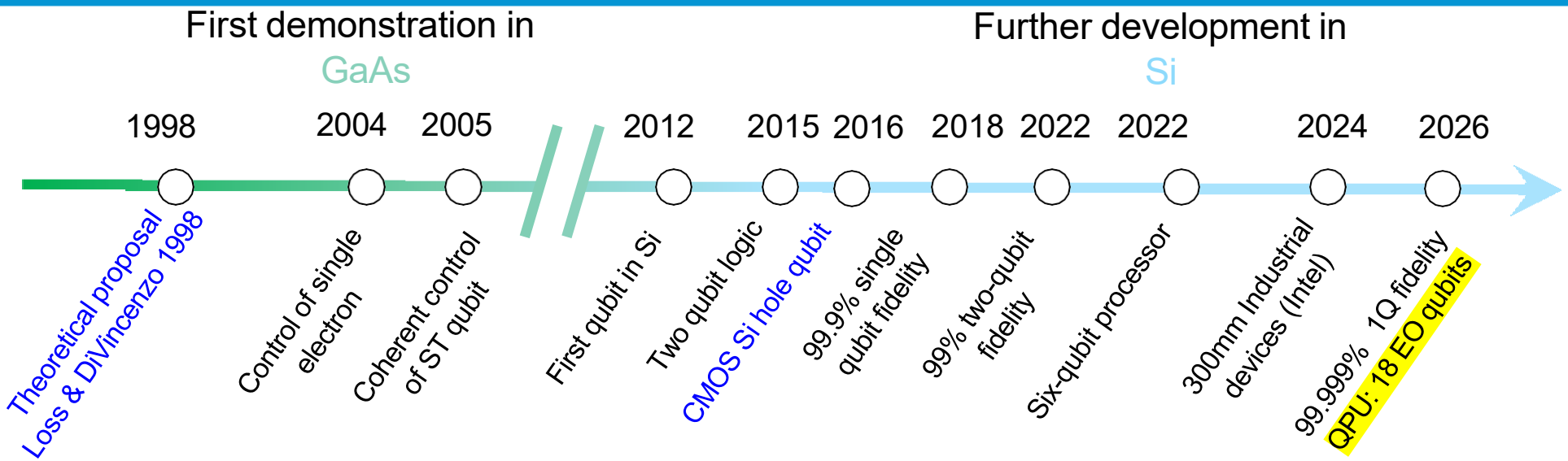
'semi-superconductor hybrids' & TIs

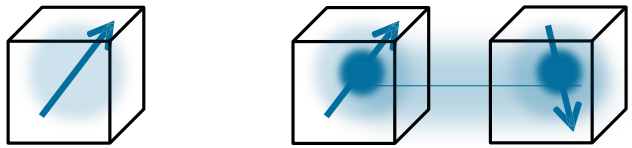
'many theorists', Microsoft

'exotic'
Majorana ?
Para- or Fibonacci fermions?

See e.g. *Nanomaterials for Quantum Information Science and Engineering*, Alfieri et al., Advanced Materials, 2109621 (2022)

History of spin qubits in quantum dots





Loss and DiVicenzo, PRA (1998)

Elzerman et al. Nature (2004)

Petta et al. Science (2005)

Maune et al. Nature (2012)

Veldhorst et al. Nature (2015)

Maurand et al. Nat. Comm (2016)

Yoneda et al. Nat. Nano (2018)

Noiri et al. Nature (2022)

Xue et al. Nature (2022)

Philips et al. Nature (2022)

Mills et al. Science Adv. (2022)

Neyens et al. Nature (2024)

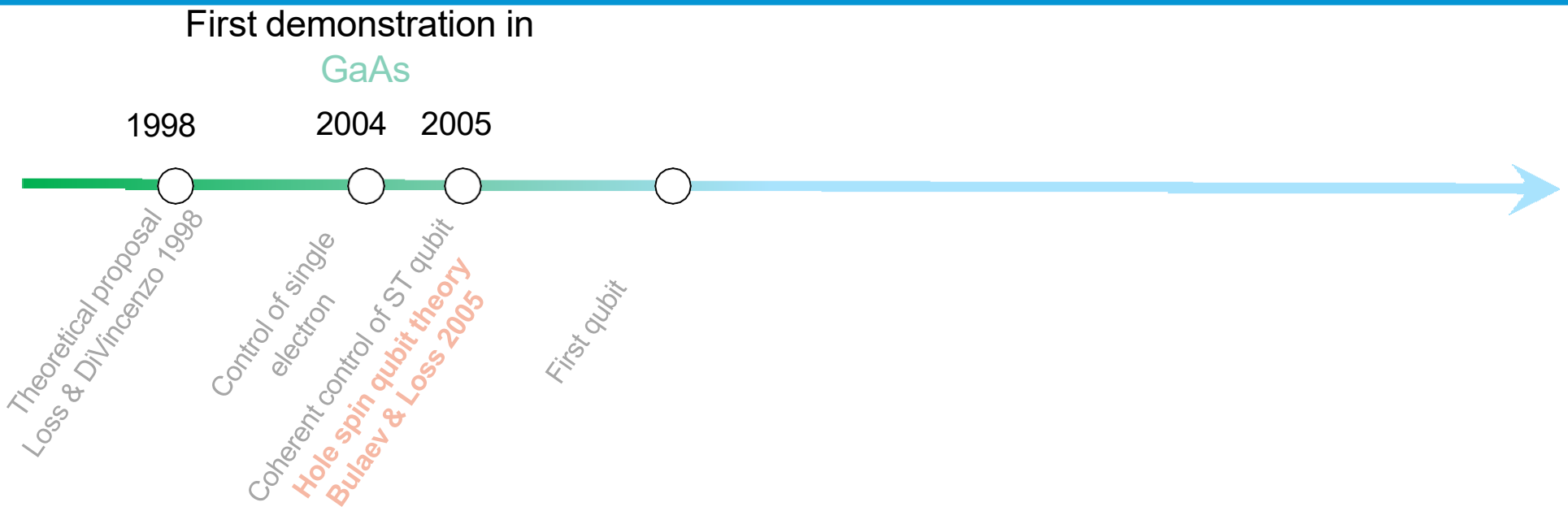
Steinacker et al. ArXiv (2024)

Wu et al., arXiv:2507.11918

HRL, Nature 655, 1154 (2026)

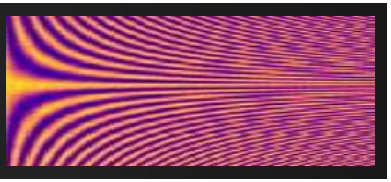
QuTech

Germanium Quantum dot spin qubits



Spin Qubit 'Zoo' in Semiconductors

Review: Burkard et al., RMP 95, 025003 (2023); McIntyre, Sarkar and DL, NJP 28, 081203 (2026)



Spin Qubit Control technology

	Si:P	^{28}Si:P MOS	^{28}Si nMOS (planar)	Si nMOS (burried channel)	Si nMOS (NW)	Si nMOS (planar)
Antenna (ESR)	UNSW	UNSW	UNSW TU Delft	TU Delft/Intel	Grenoble/LETI Cambridge Copenhagen	RIKEN /IMEC

	Si/SiGe QW	^{28}Si MOS	^{28}Si/SiGe QW		
μ Magnets (artificial SOI)	TU Delft Princeton RIKEN	UNSW	RIKEN Princeton HRL/UCLA TU Delft	Intel HRL	Tokyo/RIKEN

Loss-DiVincenzo 1998
~ 10K citations

	Si pMOS (NW)	Ge hut wire	Si pMOS (planar)	Ge QW	Ge QW	Ge QW	Si nMOS (+valley)
strong SOI (Holes) Bulaev & Loss, PRL 2005	Grenoble/LETI IMEC	IST Vienna UST China	UNSW	TU Delft	TU Delft	Groove	Grenoble/LETI

direct Rashba
Kloeffel et al. PRB 2011

Ge/Si NW	Si finFET
Basel	Basel/IBM

(and many more)

SOI: spin-orbit interaction NW: nanowire QW: quantum well

Review of performance metrics of spin qubits in gated semiconducting nanostructures

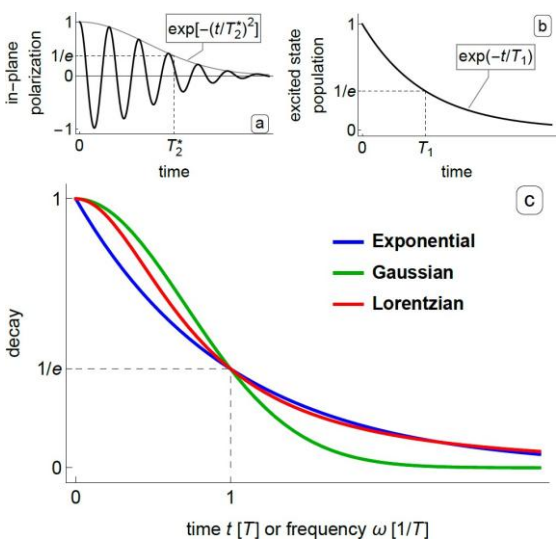
Peter Stano[1] and Daniel Loss[1,2]

[1]*RIKEN Center for Emergent Matter Science (CEMS), Wako, Saitama 351-0198, Japan*
[2]*Department of Physics, University of Basel, Klingelbergstrasse 82, CH-4056 Basel, Switzerland*

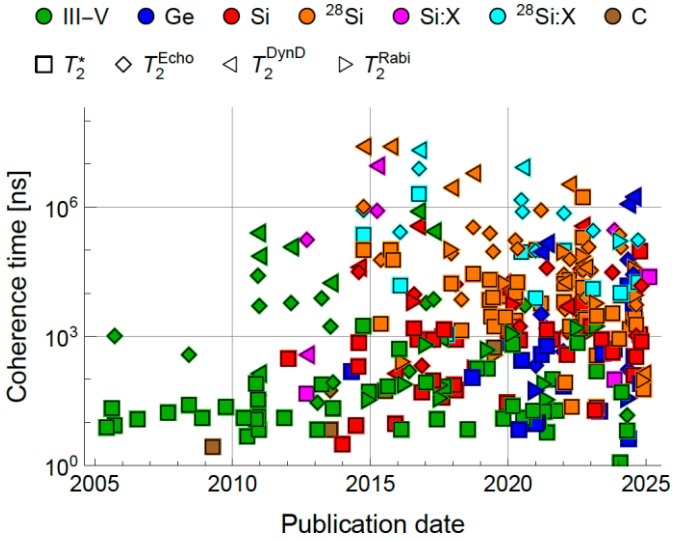
(Dated: July 15, 2021)

Nat Rev Phys 4, 672 (2022)
updates: arXiv:2107.06485v9

Spin decay times



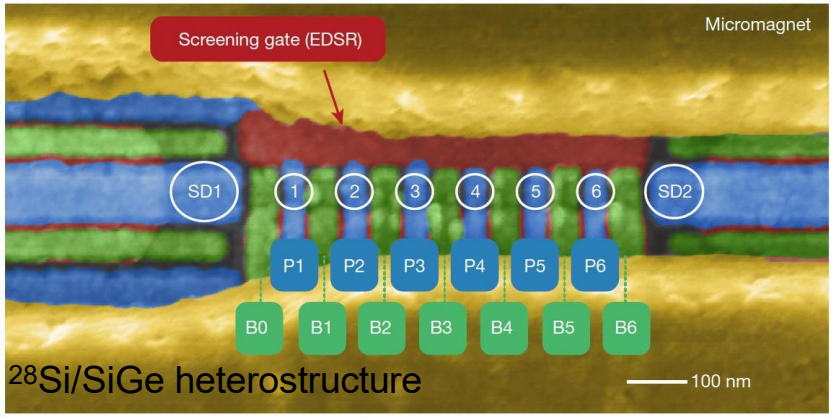
Measured spin coherence times

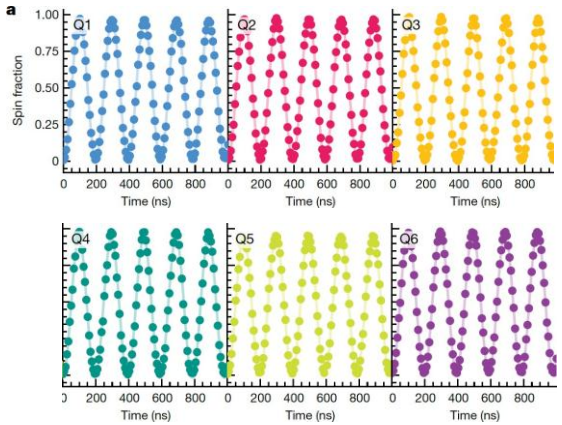


T_2^*: inhomogeneous dephasing; $T_2^{\#\$\%\&}$: Hahn echo; $T_2^{'()'}$: dynamical decoupling; $T_2^{*+,-}$: Rabi decay

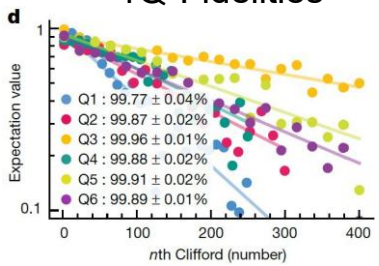
Universal control of a **six-qubit** quantum processor in silicon

Philips,...,Veldhorst, Scappucci, Vandersypen, Nature 609, 919 (2022)





1Q-Fidelities



2-3 ‘nines’

single-qubit properties:

Qubit	T_2^* (μs)	T_2^h (μs)	Vis. (%)
1	3.0 ± 0.2	14.0 ± 3.2	95.5
2	2.5 ± 0.1	21.1 ± 6.71	95.5
3	3.7 ± 0.3	40.1 ± 4.5	98.0
4	3.7 ± 0.3	37.2 ± 3.8	97.0
5	5.9 ± 0.4	44.7 ± 8.2	93.5
6	5.1 ± 0.4	26.7 ± 4.8	96.5

two-qubit gates:

Qubits	Fidelity (%)	Concurence (%)
1-2	89.2 ± 2.2	86.7 ± 3.2
2-3	90.1 ± 2.2	83.9 ± 3.8
3-4	88.3 ± 3.6	87.9 ± 5.0
4-5	95.6 ± 2.0	94.9 ± 3.2
5-6	94.1 ± 1.4	90.6 ± 3.6

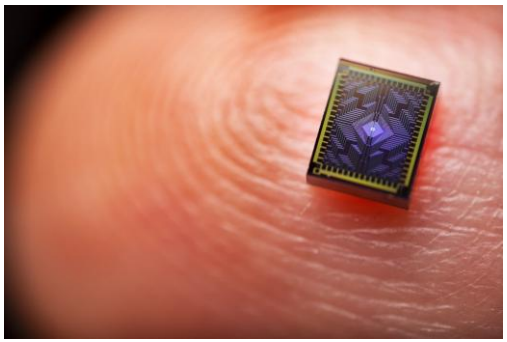
three-qubit GHZ states:

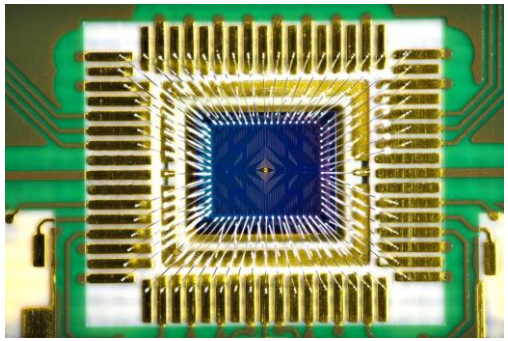
Qubits	ϕ (rad)	Fidelity (%)	Witness
1–2–3	2.41	76.8 ± 2.2	–0.327 ± 0.022
2–3–4	–0.32	71.4 ± 3.2	–0.297 ± 0.038
3–4–5	1.67	72.2 ± 4.0	–0.291 ± 0.036
4–5–6	2.68	83.6 ± 2.2	–0.380 ± 0.024

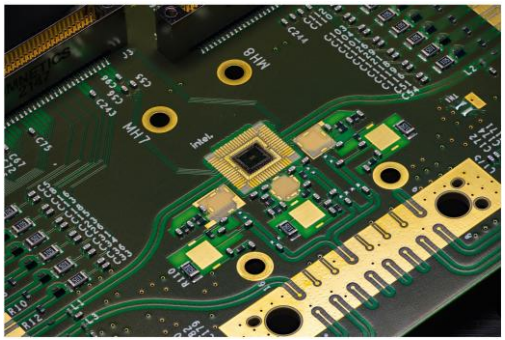
Intel: ‘Tunnel Falls’ Chip

Intel: ‘Tunnel Falls is the first silicon spin qubit device released to research institutes and universities’ (June 2023)

Neyens et al., Nature 629, 80 (2024)

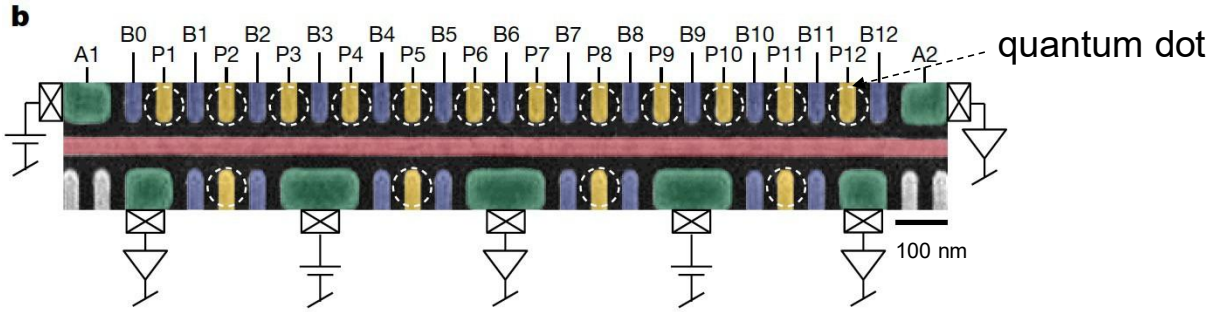






12 spin-qubit silicon chip

Si/SiGe heterostructure



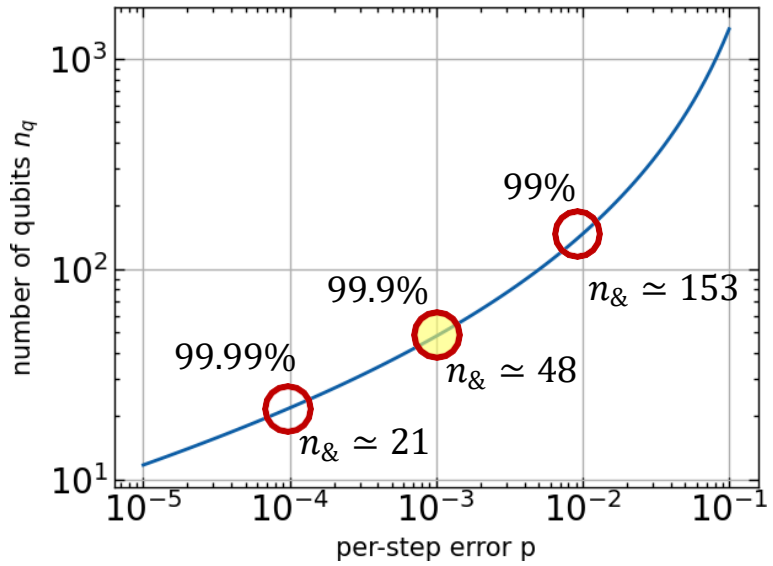
https://www.intc.com/news-events/press-releases/detail/1626/intels-new-chip-to-advance-silicon-spin-qubit-research

APS MM 2026: Intel announced a 10’000 spin qubit device

Scaling-up Qubits: Quality matters (a lot!)

# of physical qubits

$P_{"} = 10^{\#\$\%}$ **logical qubit error**



surface code threshold 0.1%
i.e. need F ≳ 99.9%

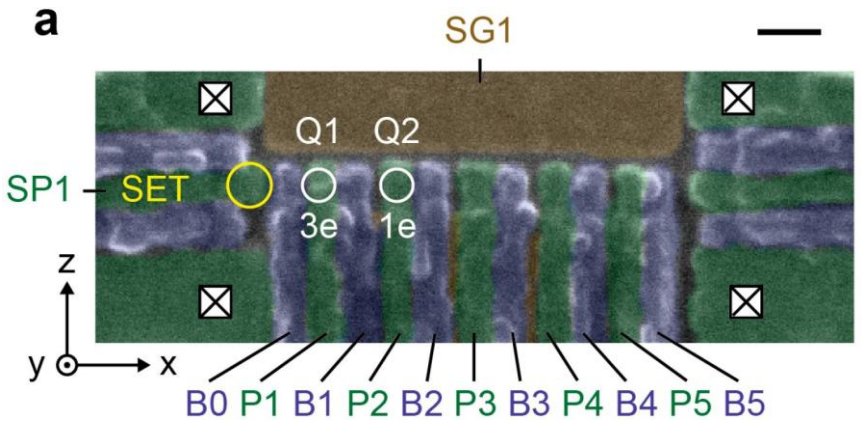
[adapted from Fowler *et al.*, PRA 86, 032324 (2012)]

Slide: Courtesy by **Yi-Hsien Wu**, Tarucha Lab, RIKEN, Japan

Single-Qubit Record: 99.999%

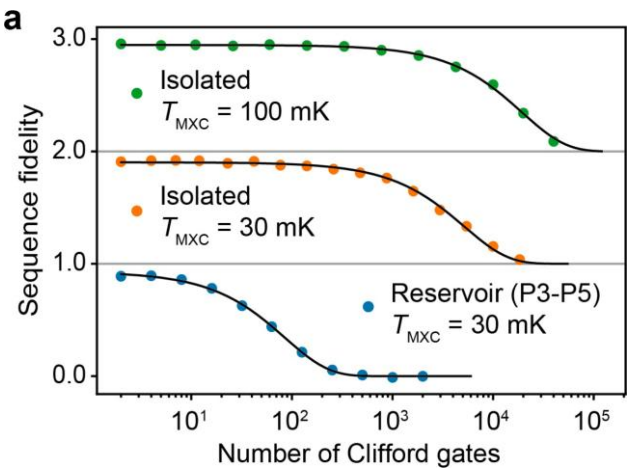
Takeda...Tarucha et al., arXiv:2608.11072

^{28}Si/SiGe



	Q1	Q2
T_2^* (μs)	3.86(2)	4.22(2)
T_2^H (μs)	90(2)	178(2)
T_2^{CPMG} (ms)	0.45(2)	0.96(3)
T_2^{Rabi} (μs)	66(11)	59(11)
$T_{1\rho}$ (ms)	0.85(8)	13.7(9)

1Q Randomized Benchmark



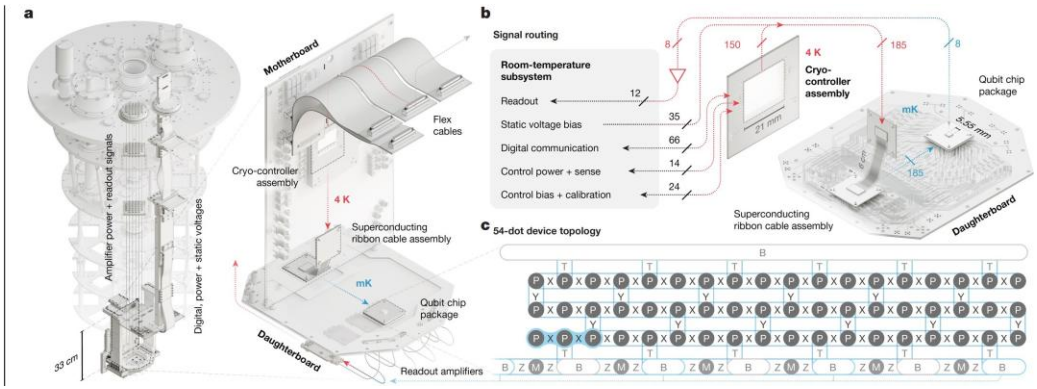
0.9999920

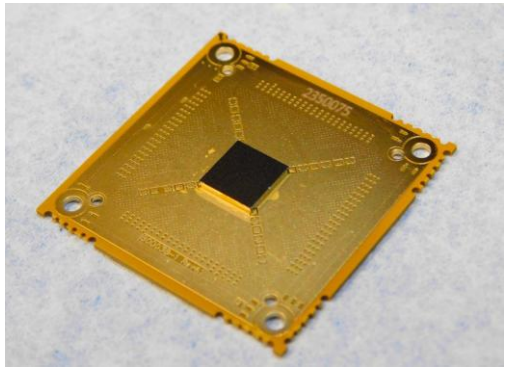
➔ qubit quality well below surface code threshold 0.1% (‘3 nines’)

A digitally controlled silicon quantum processing unit

HRL Team, Nature 655, 1154 (2026) [~250 members]

Exchange only qubit in Si: 1 EO qubit = 3 electron spins; 1Q F = 0.998, 2Q F = 0.996





QPU

QPU: 54 quantum dots in Si = 3x18 spins = 18 exchange-only (EO) spin qubits

[IBM acquired HRL Laboratories, Aug 2026]

Simultaneous operation of an 18-qubit modular array in germanium

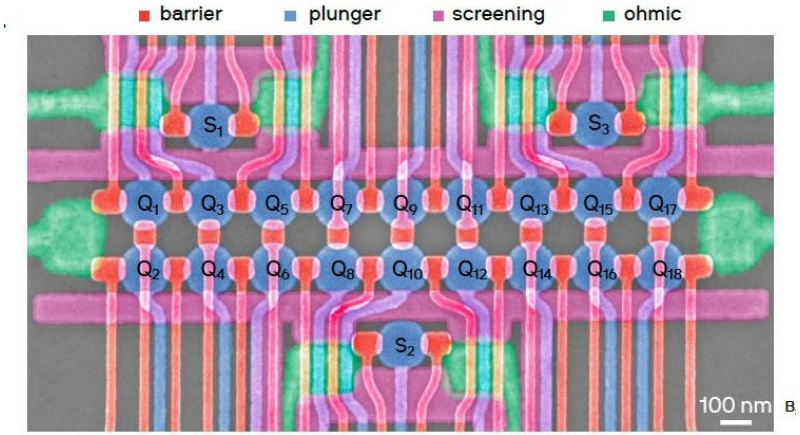
Jurgen J. Dijkema,[1,*] Xin Zhang,[1,*] Achilleas Bardakas,[1] Daniel Bouman,[1] Alice Cuzzocrea,[1] David van Driel,[1] Davide Girardi,[1] Lucas E.A. Stehouwer,[1] Giordano Scappucci,[2] Anne-Marije J. Zwerver,[1] and Nico W. Hendrickx[1]

[1] *Groove Quantum B.V., Lorentzweg 1, 2628 CJ Delft, Netherlands*

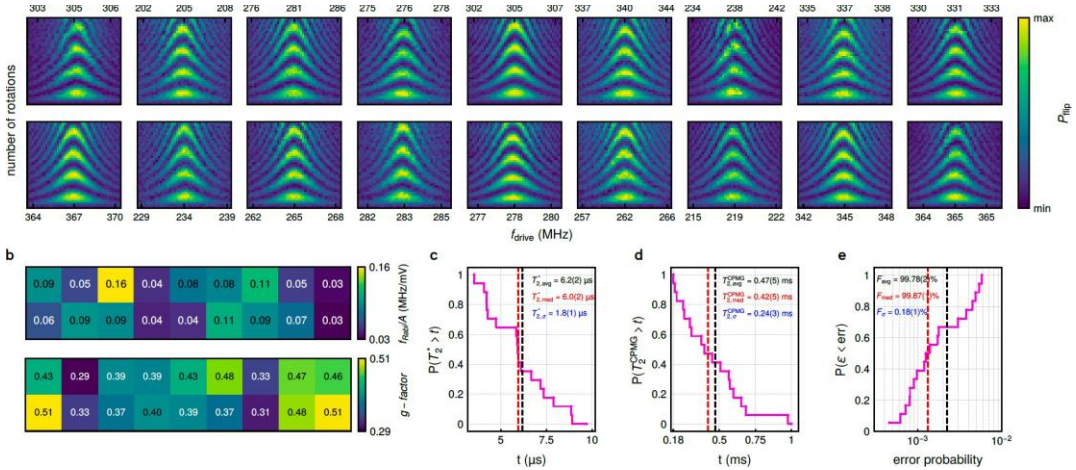
[2] *QuTech and Kavli Institute of Nanoscience, Delft University of Technology, Lorentzweg 1, 2628 CJ Delft, Netherlands*

arXiv:2604.01063

Ge/SiGe heterostructure: 18 hole spin qubits



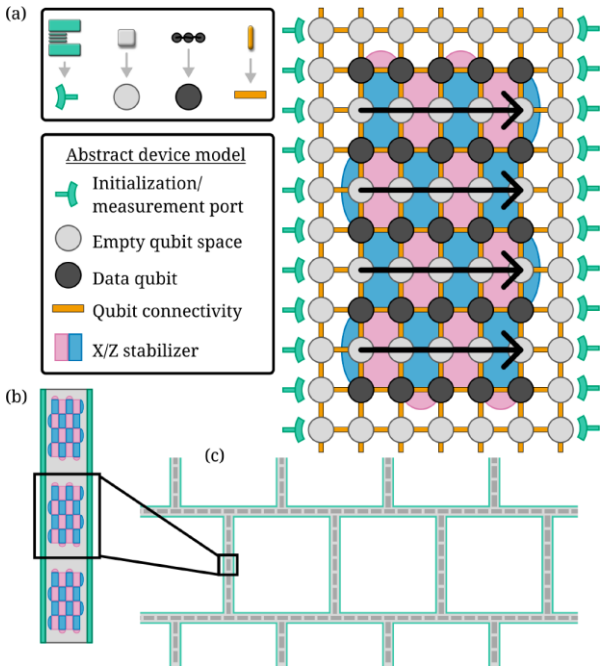
single gate fidelity: 99.9% (median)



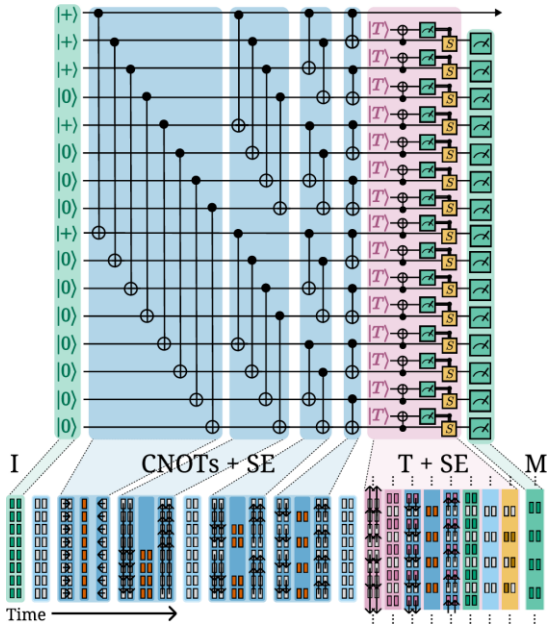
2-qubit gate fidelity?

Silicon spin qubits scalable to fault-tolerant architecture with 100 Millions of qubits ?

Recent proposal by Univ of Chicago group: Chadwick, Yang, Viszlai, and Chong, arXiv:2512.07131



Sparse architecture with shuttling links

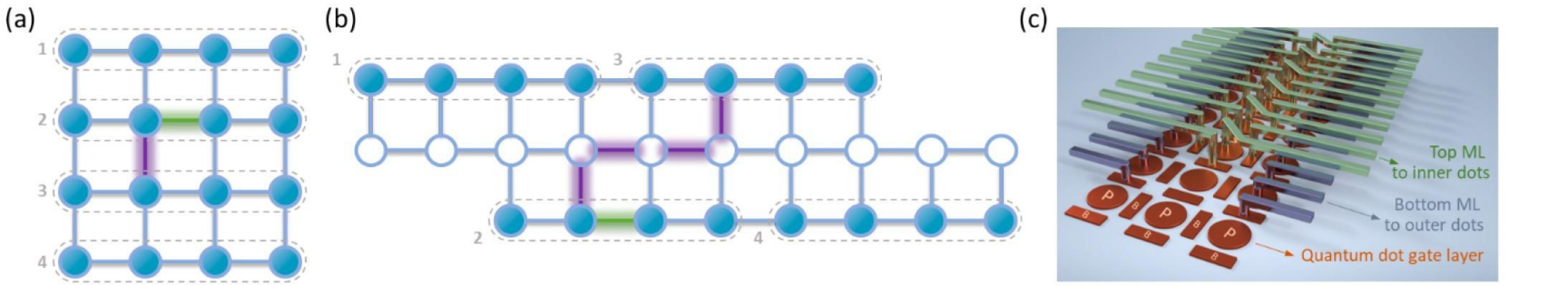


Challenge: correlated noise
Rojas et al., PR Appl 20, 054024 (2023),
arXiv:2505.05875, arXiv:2509.22073

See also Aachen/Helmholtz, Delft, Hitachi Cambridge,...

A tri-linear quantum dot architecture for semiconductor spin qubits

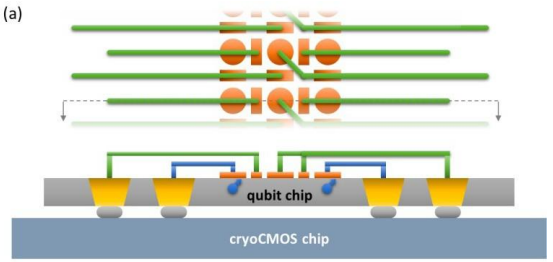
IMEC team: Li, Levajac, Godfrin, *et al.* and Greve . *Sci Rep* (April 2026). doi.org/10.1038/s41598-026-42575-z



2D quantum dot array

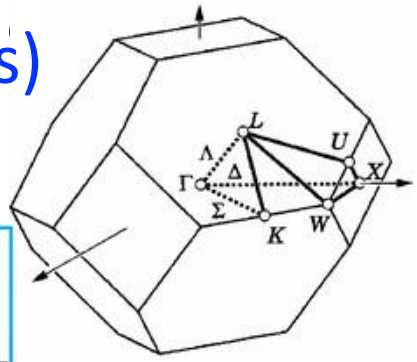
Tri-linear array with shuttling row

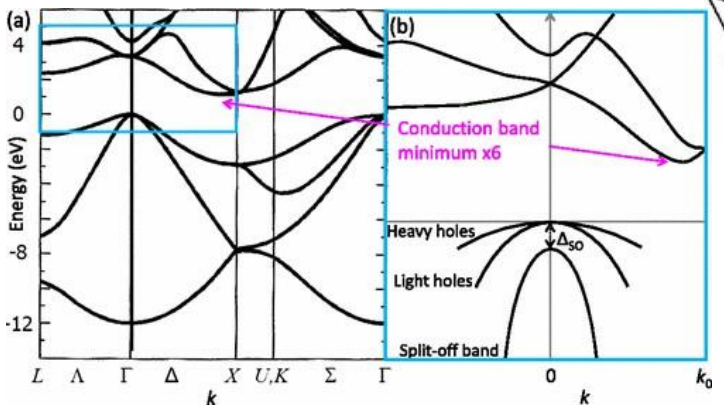
same connectivity!

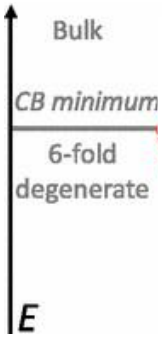


Some Issues: Valley degeneracy in Si (electrons)

- Diamond lattice with conduction band minimum close to X point
- 6-fold degeneracy in bulk Si
- In quantum well degeneracy partly lifted
- Lifting of remaining degeneracy relies on atomistic details at the interface and strong electric fields (hard to control)
- Valley splitting comparable to qubit energy







$E_{valley} \sim 200$ meV
$E_{orbital} \sim 10\ \mu\text{eV} - 100\ \mu\text{eV}$
$E_{spin} \sim 10\ \mu\text{eV}$

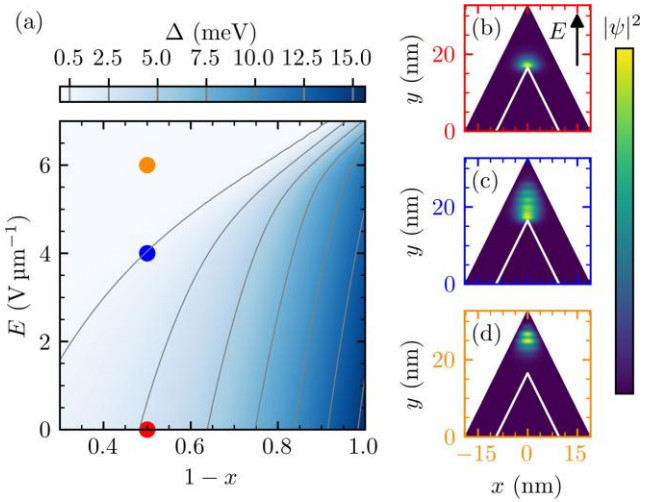
➔ valley near-degeneracy opens decoherence and relaxation channel!

Zwanenburg et al., Rev. Mod. Phys. **85**, 961 (2013)
McJunkin et al., Nat. Commun. 13, 7777 (2022)
Burkard et al., Rev. Mod. Phys. **95**, 025003 (2023)
Adelsberger, Bosco, Klinovaja, and Loss, PRL 133, 037001 (2024)

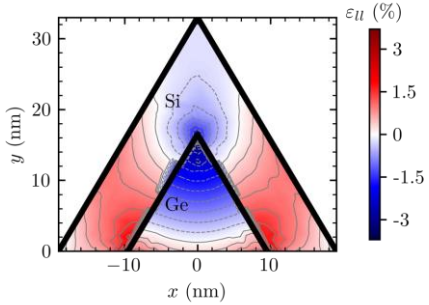
Solution: Strain Engineering Si/Si_xGe_{1-x} generates large Valley Splitting

Adelsberger, Bosco, Klinovaja, and Loss, PRL 133, 037001 (2024)

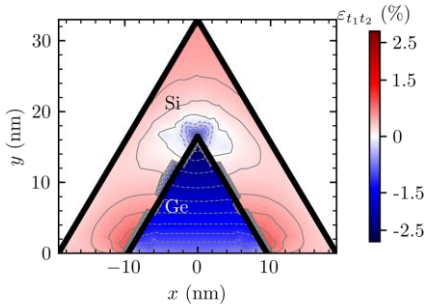
Valley splitting Δ

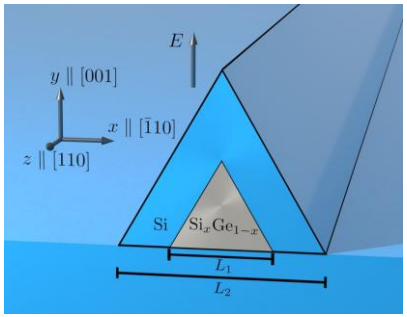


Uniaxial strain



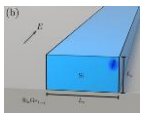
Shear strain

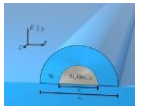




cf. *hut wires*, Gao et al., Adv. Mat. 2020; Wang et al., NanoLett 2025

- Large valley splitting
- Controllable by electric field
- Strong dependence on Ge concentration
- similar for other shapes

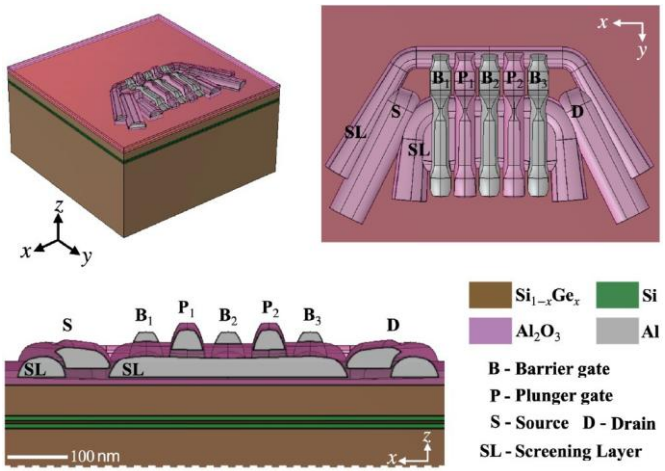




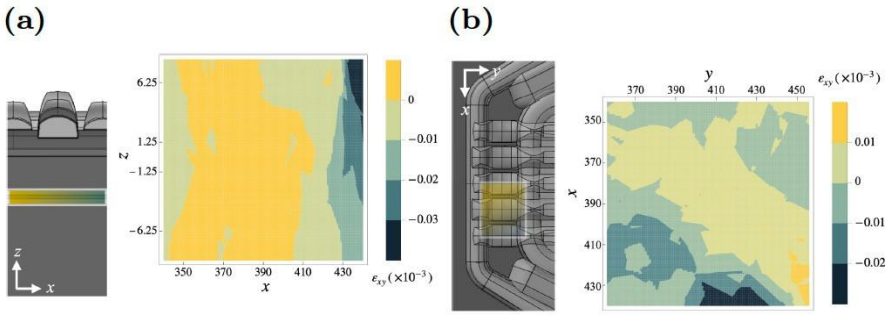
Valley splitting in Double Wells and Vertical Double Quantum Dots

Sarkar and Loss, Phys. Rev. Res. 8, 023232 (2026)

$\mathrm{Si}/\mathrm{Si}_{1-x}\mathrm{Ge}_x/\mathrm{Si}$ heterostructure



induced strain by gates and interface



➔ valley splitting ~ 200 micro eV

$$H_{\mathrm{EFA}} = \left[\frac{\hbar^2}{2}\left(\frac{(k_z + eA_z(x,y)/\hbar)^2}{m_l} + \frac{k_x^2 + k_y^2}{m_t}\right) + V(\mathbf{r}) + \Xi_u \varepsilon_{zz}\right] \mathbb{I}_{4\times 4} - 2\Xi'_u \varepsilon_{xy}\, \mathbb{I}_{2\times 2}\, \tau_z.$$

$$H_{\sigma\tau} = \left(V(\mathbf{r}) e^{-2ik_0 z}\, \mathbb{I}_{2\times 2} + 2\beta_0 (k_+ \sigma_+ + k_- \sigma_-) e^{2i(2\pi/a_{\mathrm{Si}} - k_0)z}\right) \tau_- + h.c.,$$

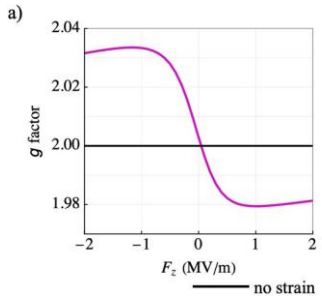
valley splitting term due to 'Ge spike'

Woods, Losert, Joynt, Friesen
arXiv:2412.19795

Electric control of LD Spin Qubits in Si Vertical Double Quantum Dots

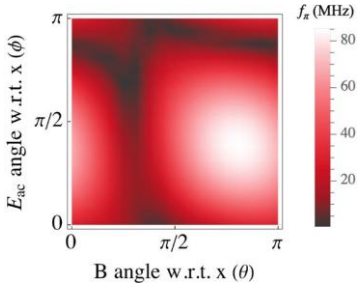
Sarkar and Loss, Phys. Rev. Res. 8, 023232 (2026)

g factor variations ➔ E(D)SR

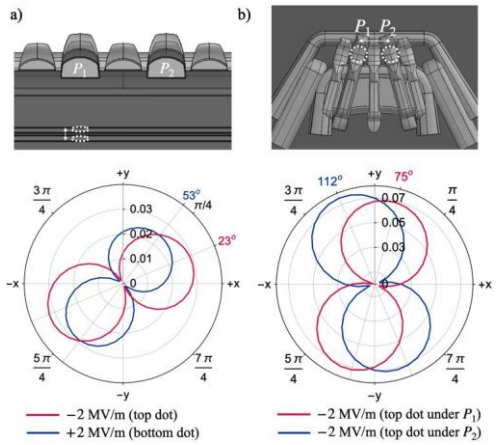


'vertical EDSR' E_z

'horizontal EDSR' E_x

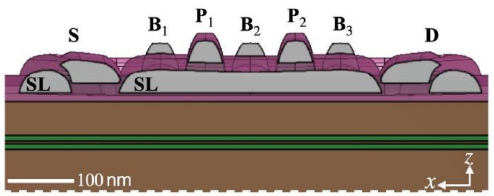


g tensor: main axis rotates

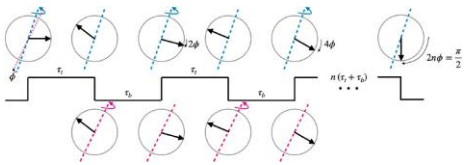


upper (left) dot
lower (right) dot

$Si/Si_{1-x}Ge_x/Si$



electric spin
control by hopping*
➔ T_g ~ 0.6 ns



📠all-electrical control of LD spin qubit in Si 📠no need of micromagnets 📠scalable

* Wang et al., Science 385, 447 (2024), Unseld et al., NC 16, 5605 (2025)

Summary

- electrons and holes in Si, Ge, and GeSn quantum dots
- classical reversible computing with spin qubits

Thanks to:

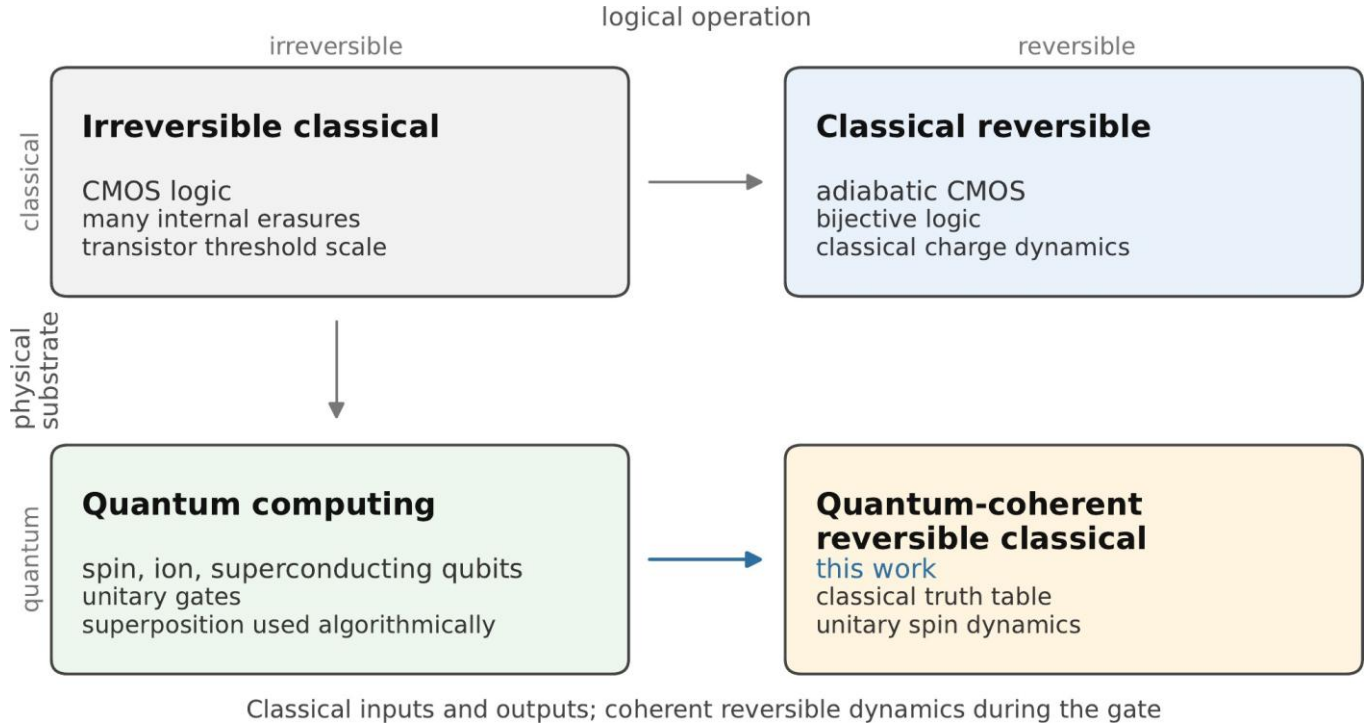
Stefano Bosco
Bence Hetenyi
Jelena Klinovaja
Ji Zou
Abhik Sarkar
Zoe McIntyre

Riken:
Peter Stano
Juan Rojas

Seigo Tarucha
Giordano Scappucci
Dominik Zumbuhl
Leon Camenzind
Giorgos Katsaros
Menno Veldhorst
Stuart Parkin

Classical Reversible Computation by Quantum Coherence

DL, arXiv:2607.06219 (2026)



THE use case

➔ classical inputs and outputs — coherent spin dynamics only during the gate

The Energy Cost of Computing Explodes (AI)

Landauer (1961): erasing one bit costs at least $k_B T \ln 2$

the Landauer scale $k_B T \ln 2$:

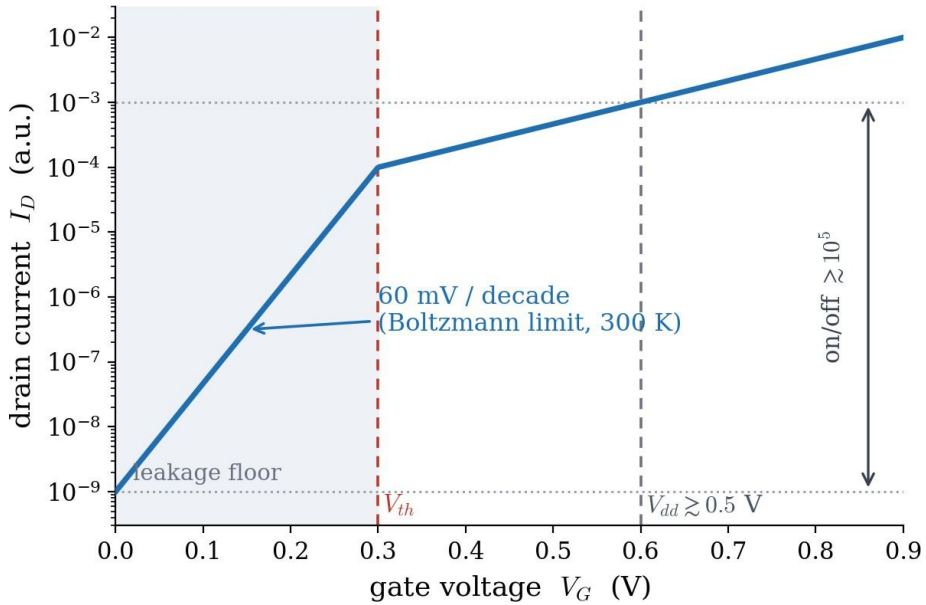
100 mK	9.6×10^{-25} J
4 K	3.83×10^{-23} J
300 K	2.87×10^{-21} J

- energy floor set by **irreversibility** (erasure) — not by computation
- But: Bennett (1973): **reversible** logic erases nothing ➔ no floor at all

➔ Is there post-CMOS platform that lowers energy cost?

CMOS floor: ‘Boltzmann tyranny’ ➔ ~10 aJ per switch

Frank & Edwards, APL Electron. Devices 1, 030902 (2025); Datta et al., Science 378, 733 (2022)



$$S = \frac{k_B T}{q} \ln 10 \approx 60 \text{ mV/decade} \quad (300 \text{ K})$$

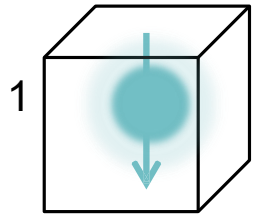
subthreshold slope ≥ 60 mV/decade at 300 K ➔ $V_{dd} \gtrsim 0.5$ V

a switch costs ~10 aJ ≈ $3 \times 10^3 \times k_B T \ln 2$

☝ set by thermal statistics (not fabrication); adiabatic CMOS uses same transistors

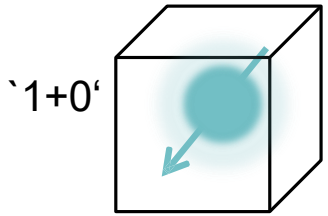
Use spins as classical bits & coherence only inside the gate

DL, arXiv:2607.06219 (2026)



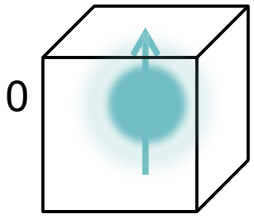
idle / shuttle
limited by T_1

classical bit in



Quantum Gate U
coherence needed (T_2)

superposition



idle / shuttle
limited by T_1

classical bit out

$$N_{\mathrm{ops}} \sim T_1/t_{\mathrm{gate}}$$

$N_{ops} \approx 1.9 \times 10^5$ gates per T_1
(dilution-fridge T_1; the 4 K value is test (vi))

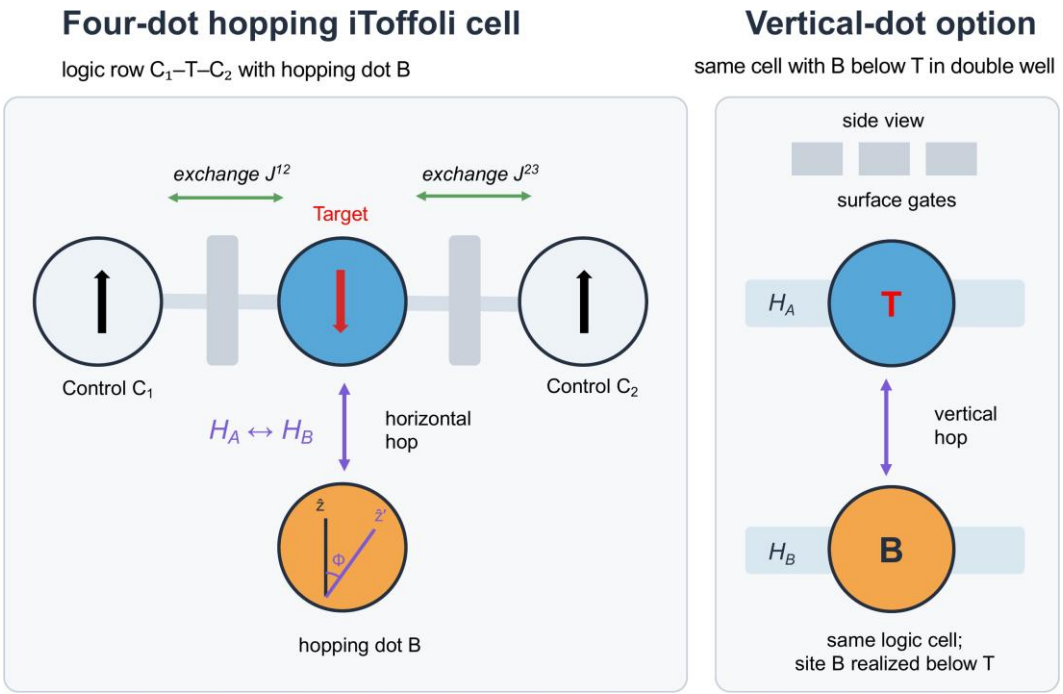
$T_1 \approx 32$ ms in Ge hole dots
Lawrie et al., 2020

➔ in- and outputs are classical states - superposition only inside U

➔ storage and transport are T_1-limited - coherence needed only during the gate

iToffoli: Universal Gate

DL, arXiv:2607.06219 (2026)



- C_1–T–C_2 chain; target hops A ↔ B
- spin axes tilted by Φ = 44.7°
- all-DC detuning pulses — baseband, no microwaves*

hopping gates: Wang et al., Science 385 (2024)

➔ iToffoli ≡ Toffoli for classical data ➔ universal reversible logic

*EDSR iToffoli: Hendrickx et al., Nature 591, 580 (2021) and Takeda et al., Nature 608, 682 (2022)

Energy Cost of Spin iToffoli

dielectric loss per hop (baseband):

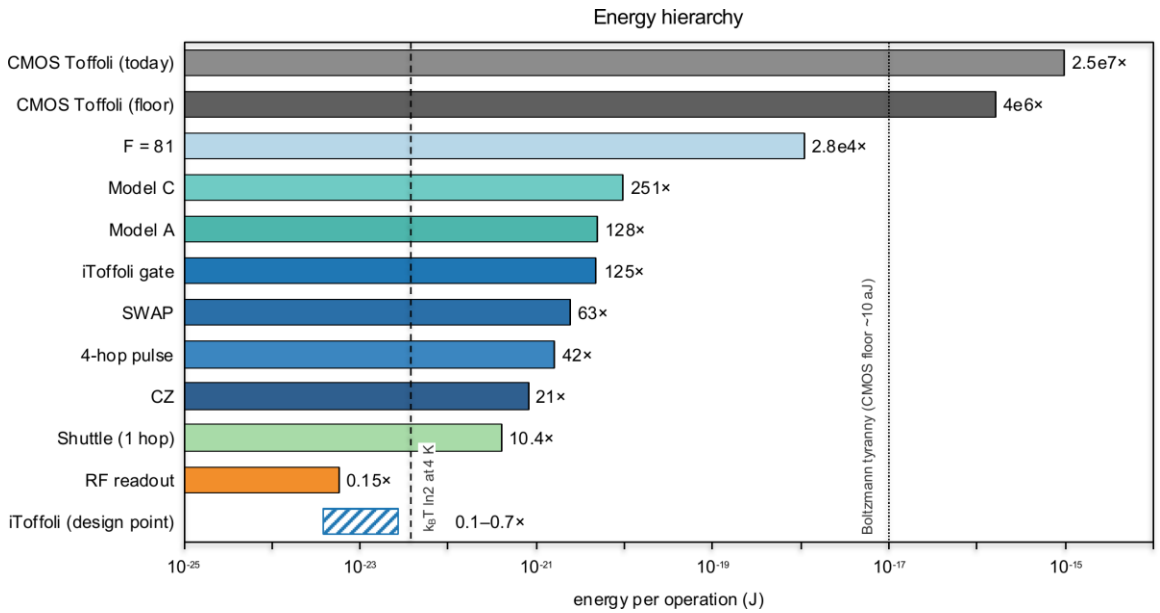
$$E_{hop} = C_g \tan\delta\,(\Delta V)^2$$

Wang et al., Science (2024)

ΔV = 20 mV & 12 hops/gate

$E_{gate} \approx 4.8\times10^{-21}$ J ≈ 125 $k_B T \ln 2$ (4 K)

about 100× the 4 K Landauer scale



~$2\times10^5\times$ demonstrated vs. CMOS today

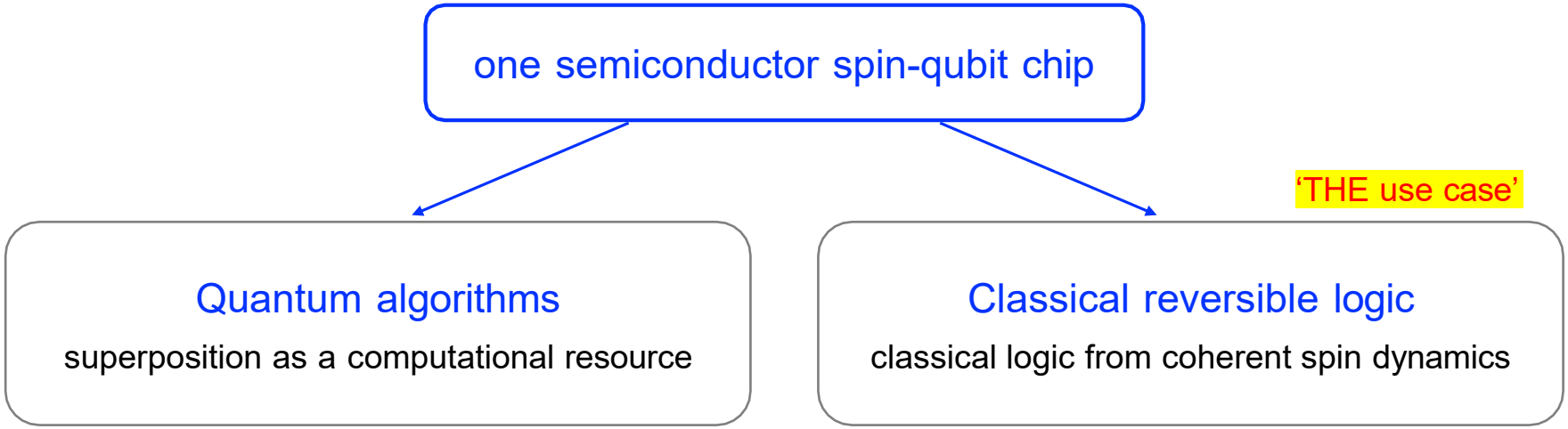
~$10^7\times$ design point vs. the CMOS floor

~$10^{3–4}\times$ at the wall plug, device term

➔ the advantage survives at system level (~$10^4\times$ at F = 81) — error correction is a classical vote

One chip, two roadmaps

DL, arXiv:2607.06219



➔ dissipation set by dielectric loss, no thermodynamic floor ➔ 5-7 orders below CMOS at device level

➔ quantum computing & low-energy post-CMOS in same platform

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