



SCALABILITY & COST COMPETITIVENESS:

**How semiconductors pave the way to commercializable
quantum computers**

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Quobly in 2026

Headquarters in Grenoble, France
Spin-off in 2022 from



€10M

Revenue
First commercial contract
through PROQCIMA

65

Patents families

120+

People

x3

By mid 2028

54%

PhDs

20

Nationalities

5

Locations

Grenoble FR (HQ)
Paris FR
Sherbrooke CA
Singapore
Taiwan

25+

partnerships

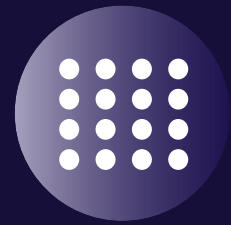


Exclusive partnership to
develop our proprietary
QSOI® qubit technology
and produce million-
qubit chips

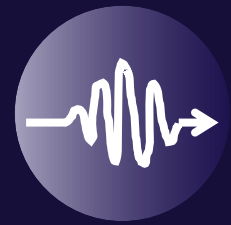
June 2026: Quobly secures 115M€

Quantum computing bottleneck is industrialization

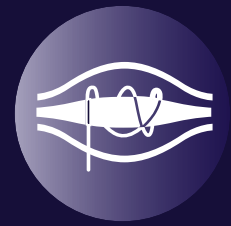
Current early quantum technologies



Neutral atoms



Photons

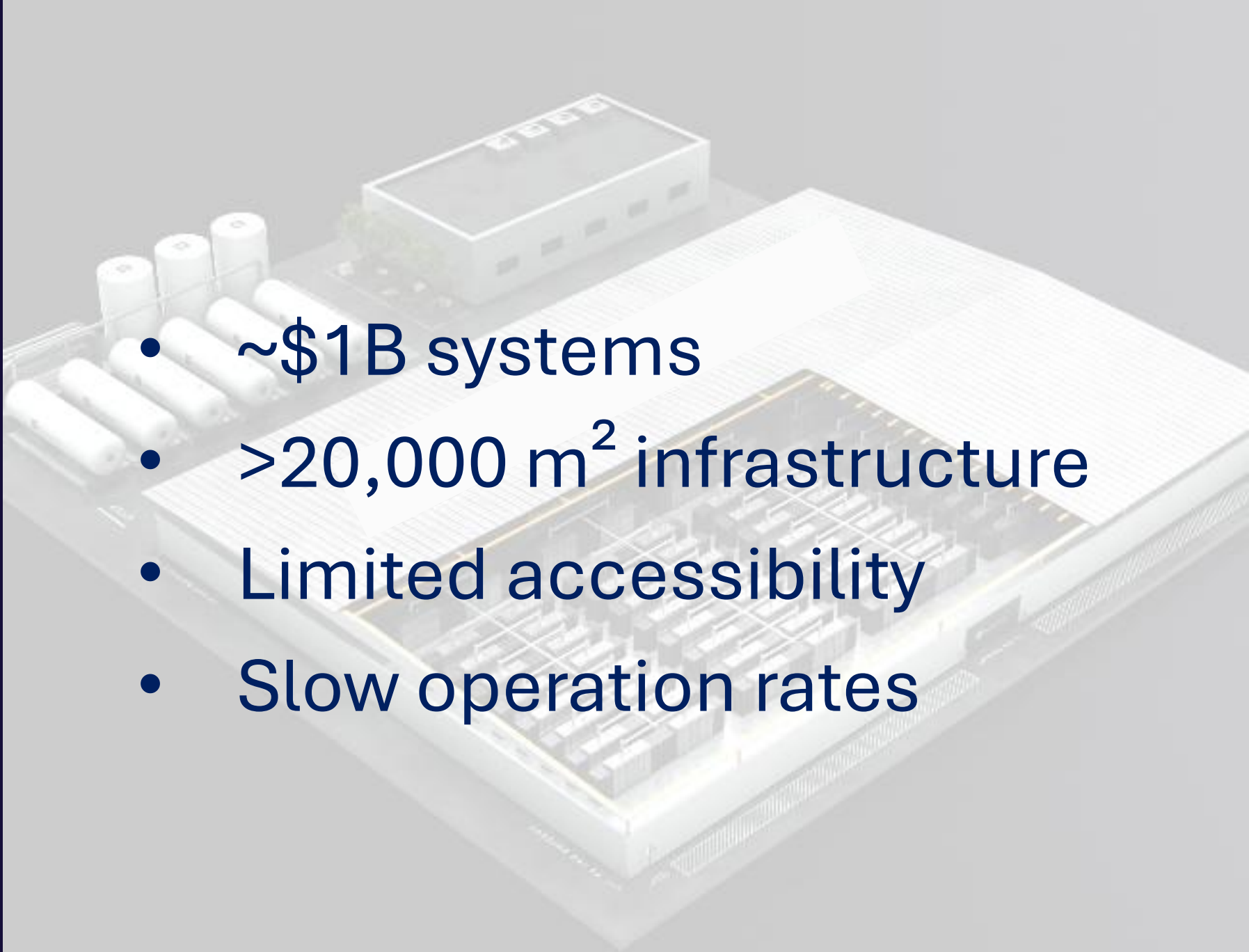


Trapped ions



Superconductors

are limited in terms of delivering
value to the customers

- 
- ~\$1B systems
 - >20,000 m² infrastructure
 - Limited accessibility
 - Slow operation rates

Introducing the Alloy product line

Value proposition: by 2032, data center ready million qubits quantum computer



1M qubits
on 1 single
chip

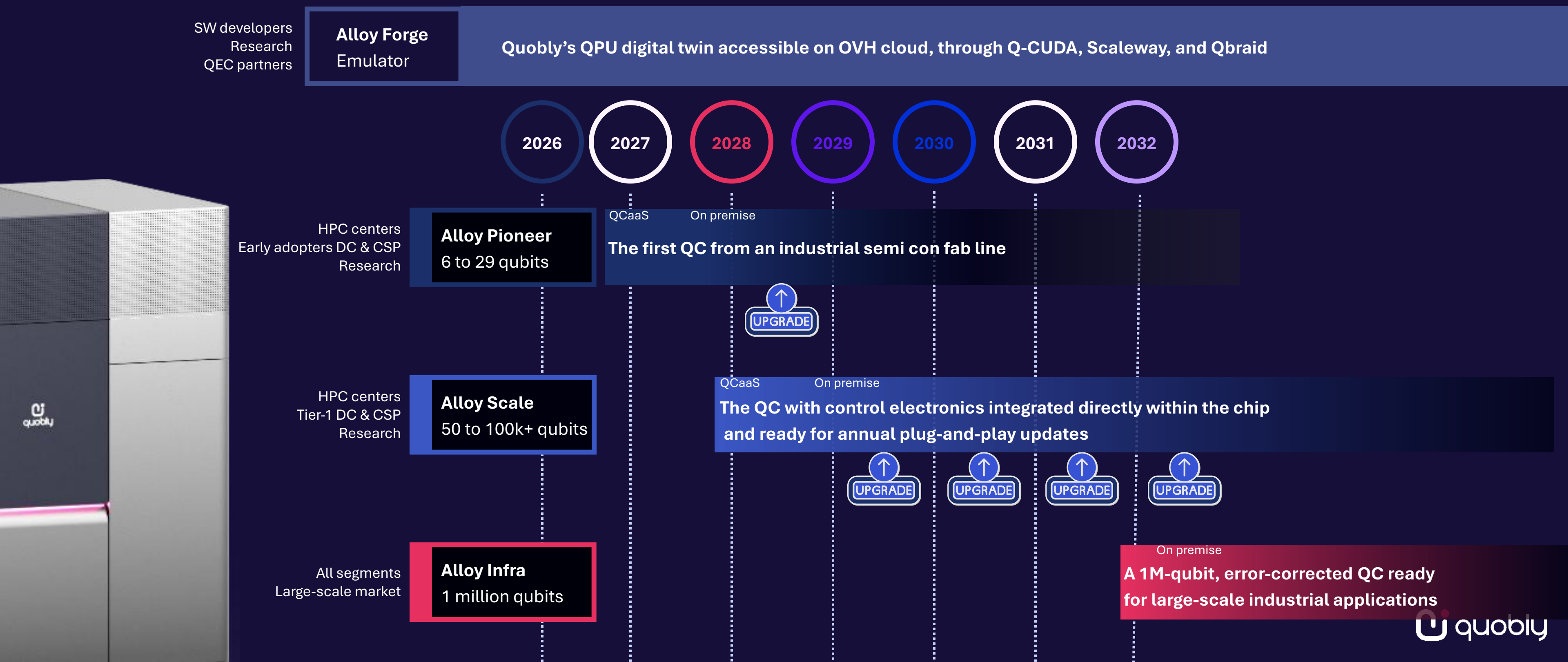


10m² quantum computer compatible with HPC and data centers for pervasive hybrid quantum-classical computing

1,000x faster, **100x** smaller, **10x** cheaper

The Alloy product line: designed for existing data centers

A continuous industrial scaling path with PnP upgrades



Building quantum processors on the semiconductor industry

- Silicon-based quantum processors
- Proprietary qubit **QSOI®** technology manufactured in **STMicroelectronics commercial fabs**
- **Co-integrated with industrial FD-SOI** transistor technology to scale control
- **Fabless model** using same semiconductor fabs as advanced transistor technologies (\$Bs in CAPEX and quarters-to-industrialization saved)
- **System vision** thanks to hardware-software accelerated co-development with PDKs and SDKs

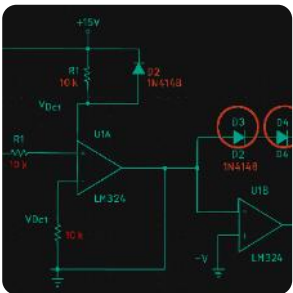
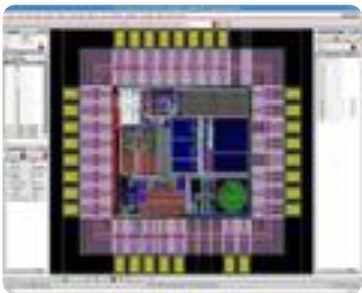
Industrial life cycle of a Quantum Chip



1

Design

Quobly designs the circuit through iterative simulations and layout
A GDS⁽¹⁾ file is then sent to ST for fabrication



2

Wafer fabrication

ST fabricates the chip based on Quobly's proprietary design (GDS) and process flows on 28Si industrial grade wafers

Worldwide unique industrial grade 28Si SOI wafers supply chain



purifies SiF₄ to get 99.99% pure Silicon isotope 28 (Si28)

transforms SiF₄ into SiH₄ ready for Silicon epitaxy process

transforms SiH₄ into a crystalline Silicon layer and use it to manufacture a Si28 purified FDSOI wafer



ST manufactures wafers and delivers them to Quobly when fabrication flow is complete



3

High-added value low temperature statistical characterization

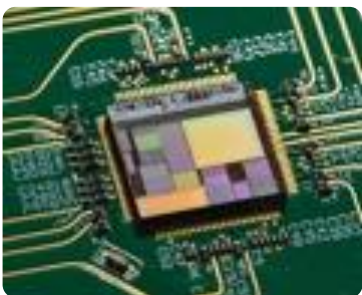
Quobly has developed a unique expertise in performing room temperature and cryogenic temperature tests to develop high-performance QSOI® technology



4

Final performance validation

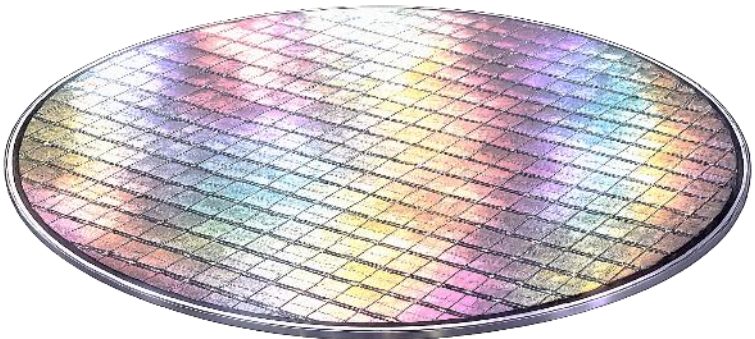
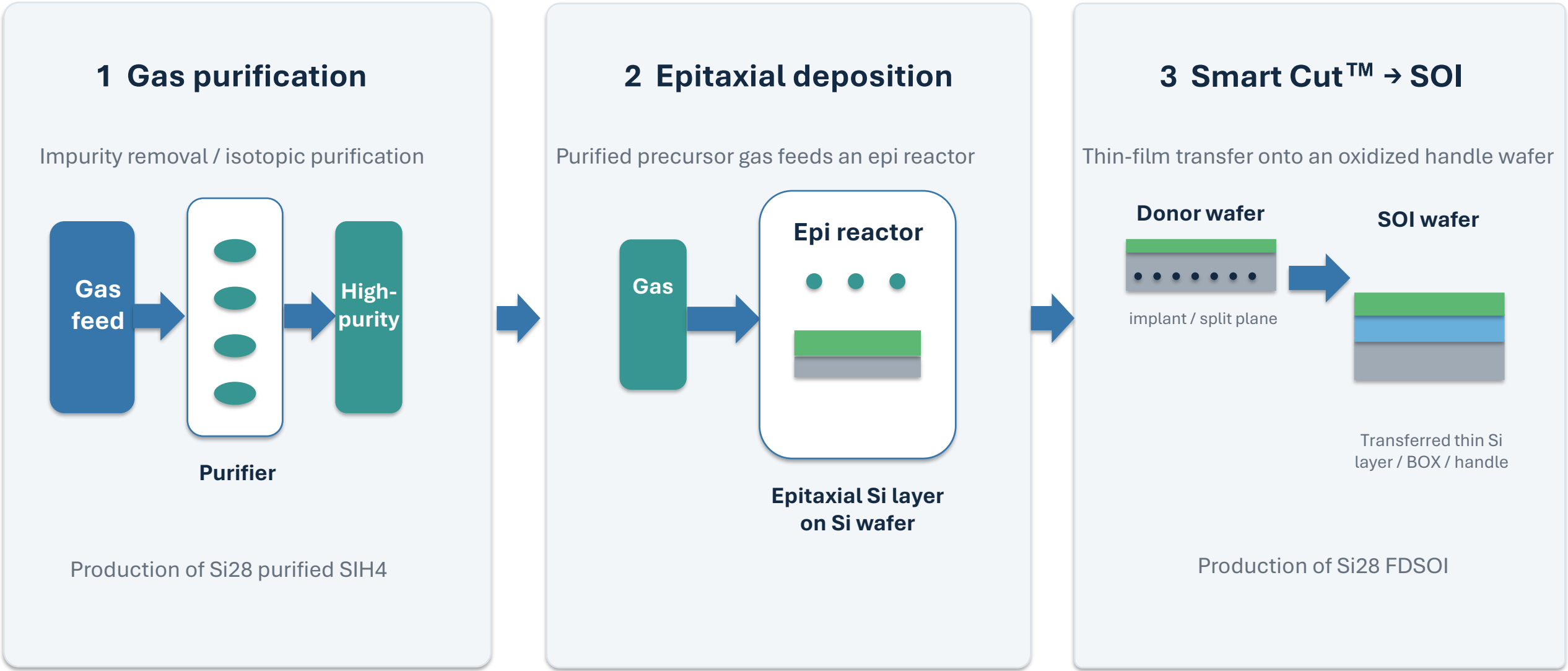
After dicing, qubit chip performance is validated in cryostat



⁽¹⁾ Graphic Data System

Completion of the full cycle in our industrial environment

Orano, Air liquide, Soitec and ST have completed the cycle in January 2026

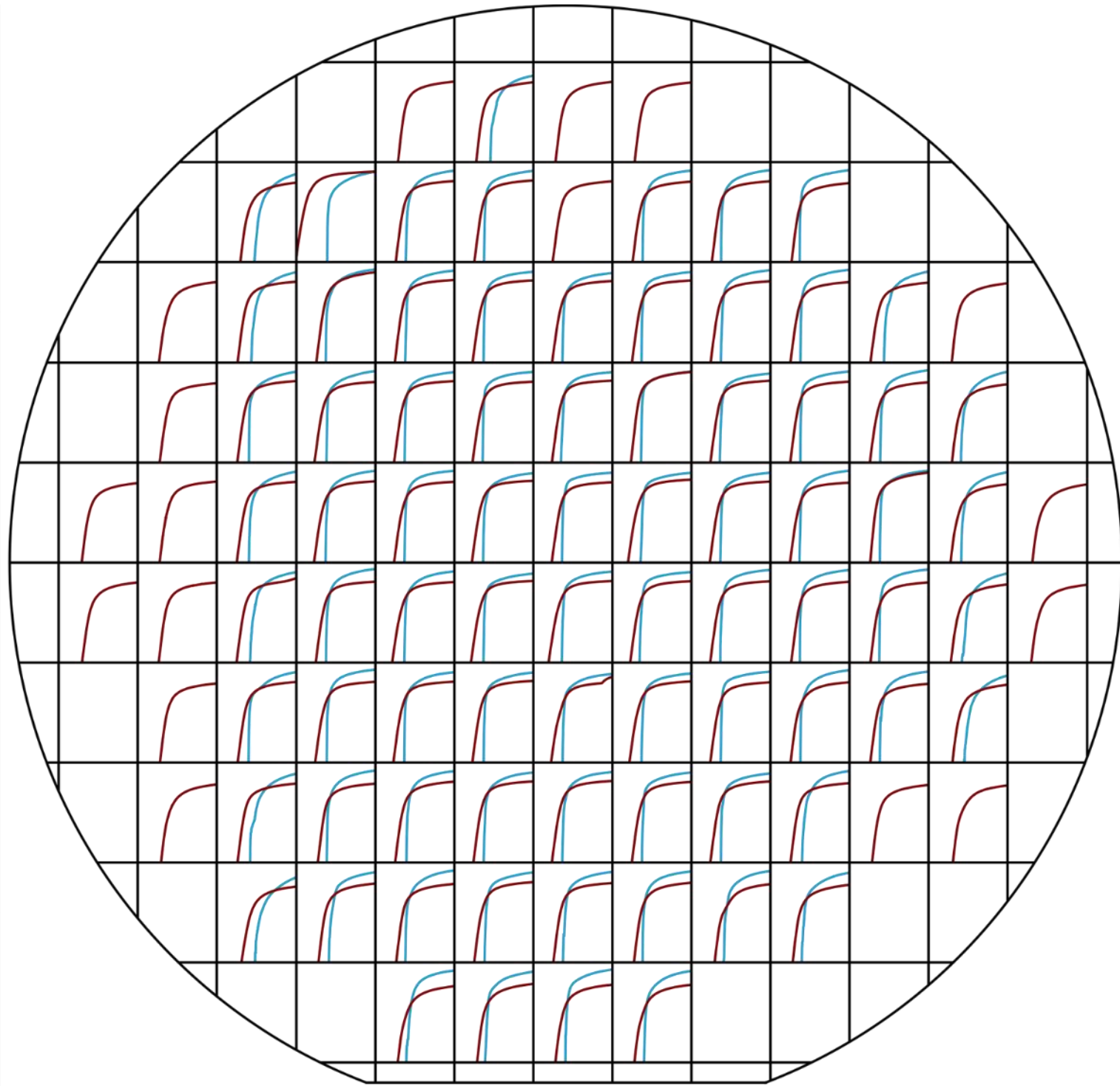


QSOI® on isotopically pure Si28 layer

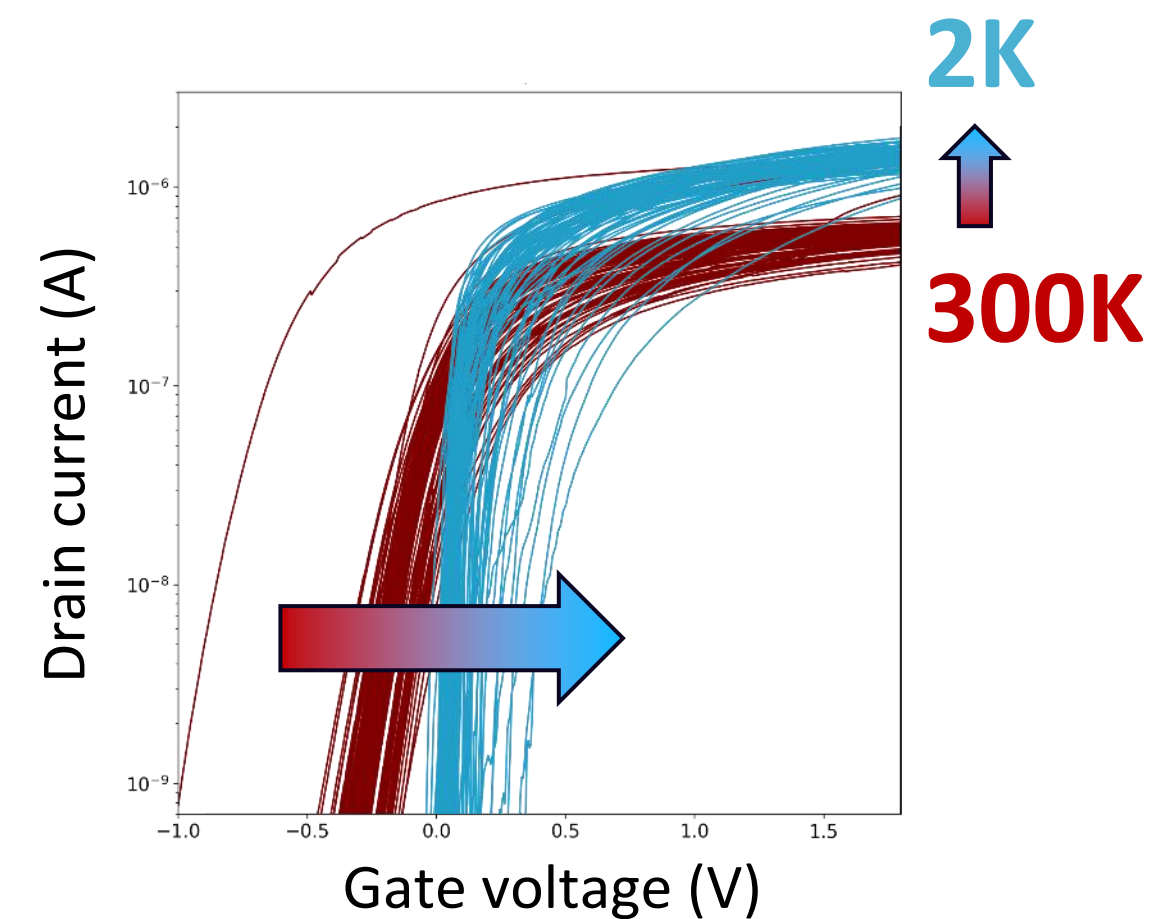


Qubit device characterization (**300K** and **2K**)

Wafer throughput for statistical analysis is higher at 300K due to the cooling time ($\approx 150\text{min}$) required to reach 2K.

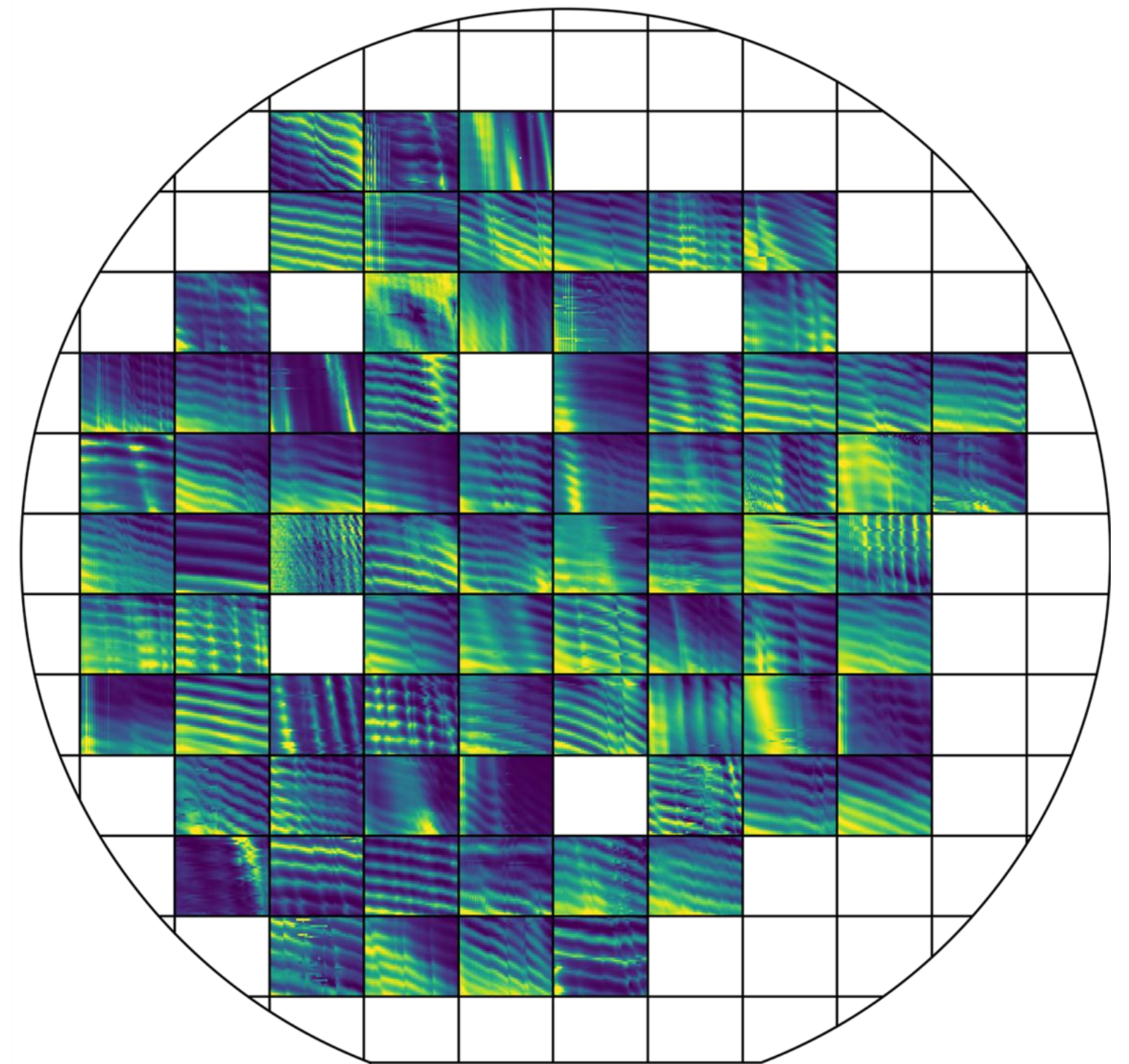
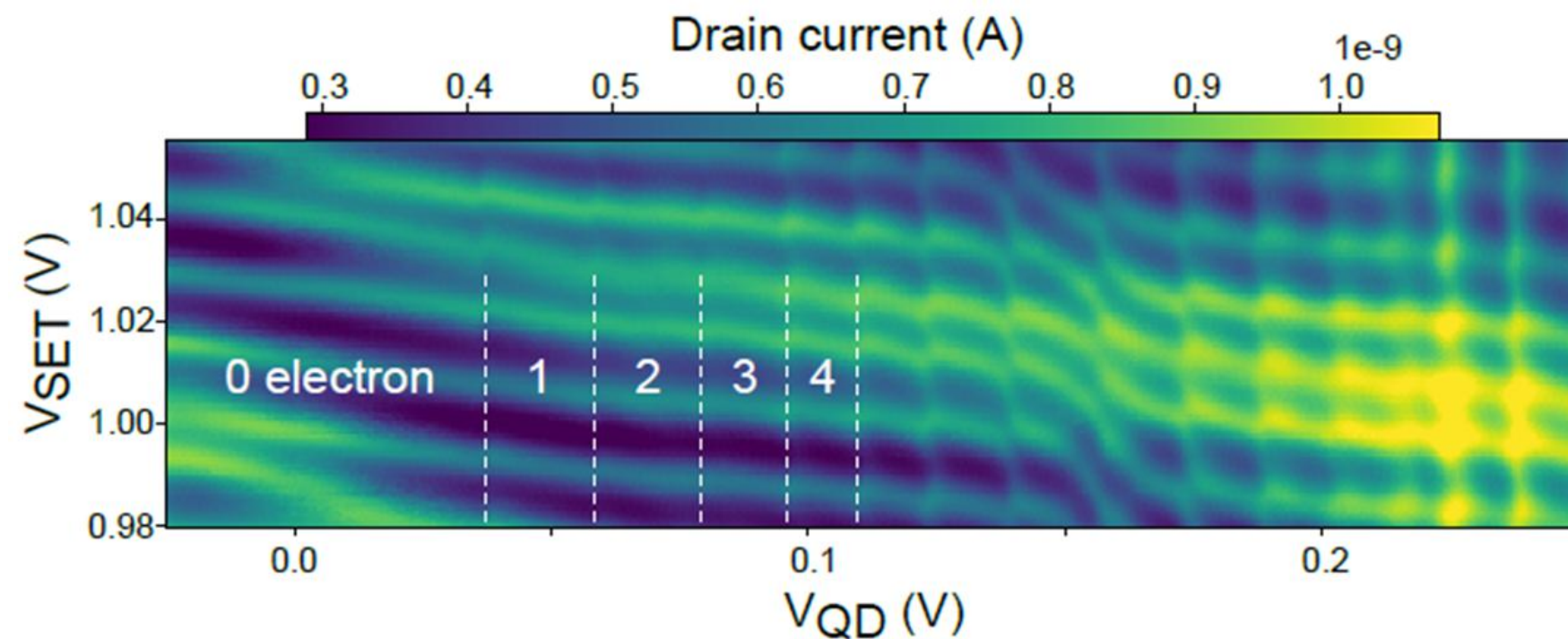
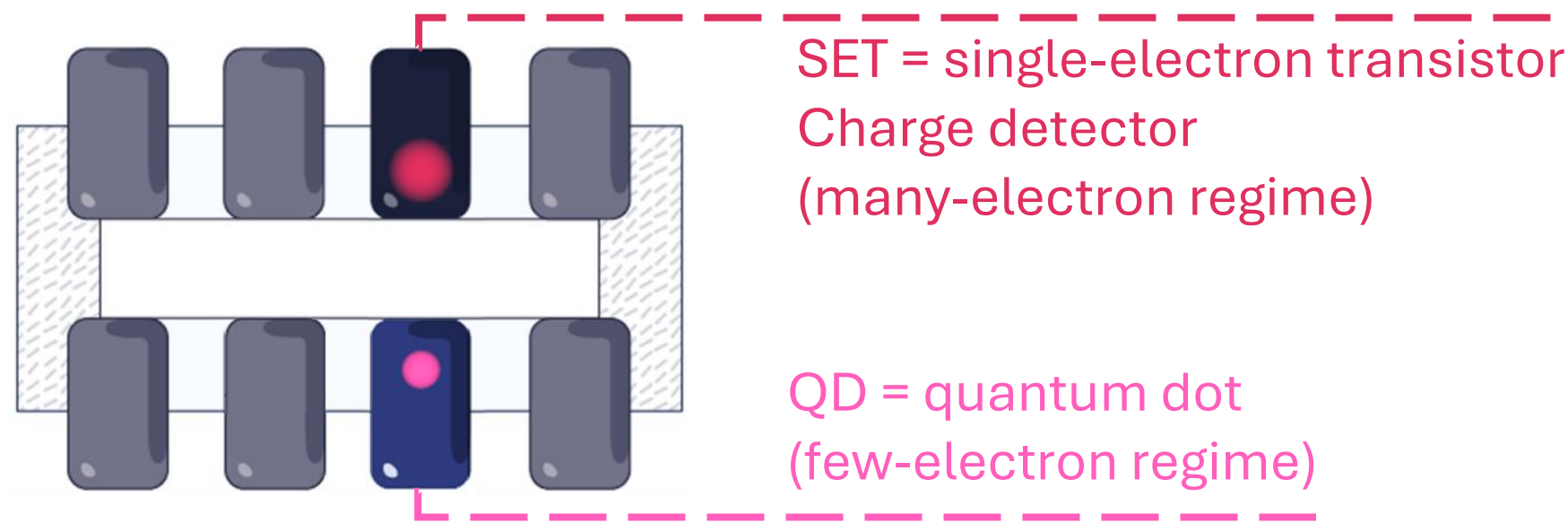


Time to measure 784 IV curves:



Qubit device characterization (2K): QD performance

Charge detection

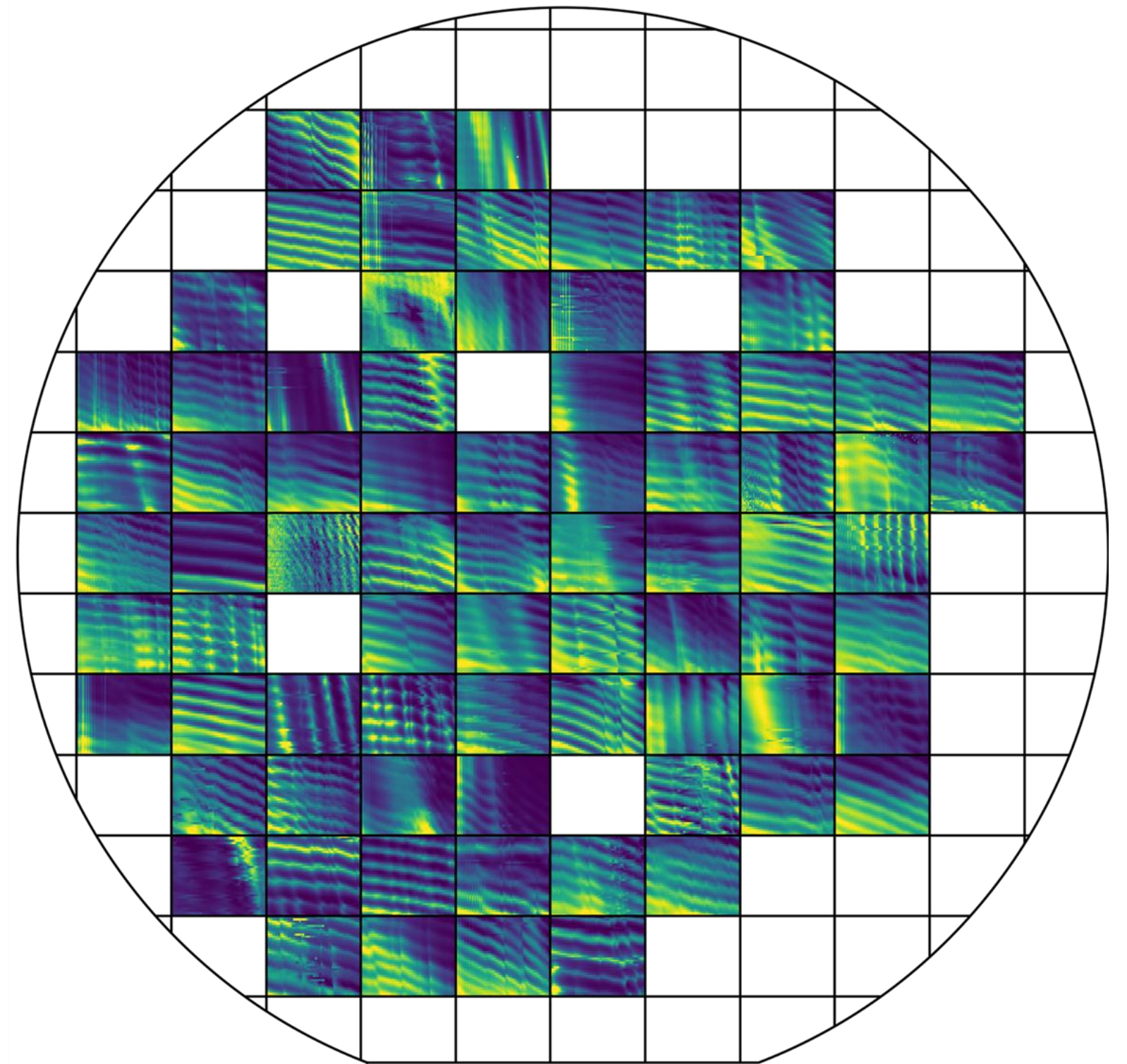
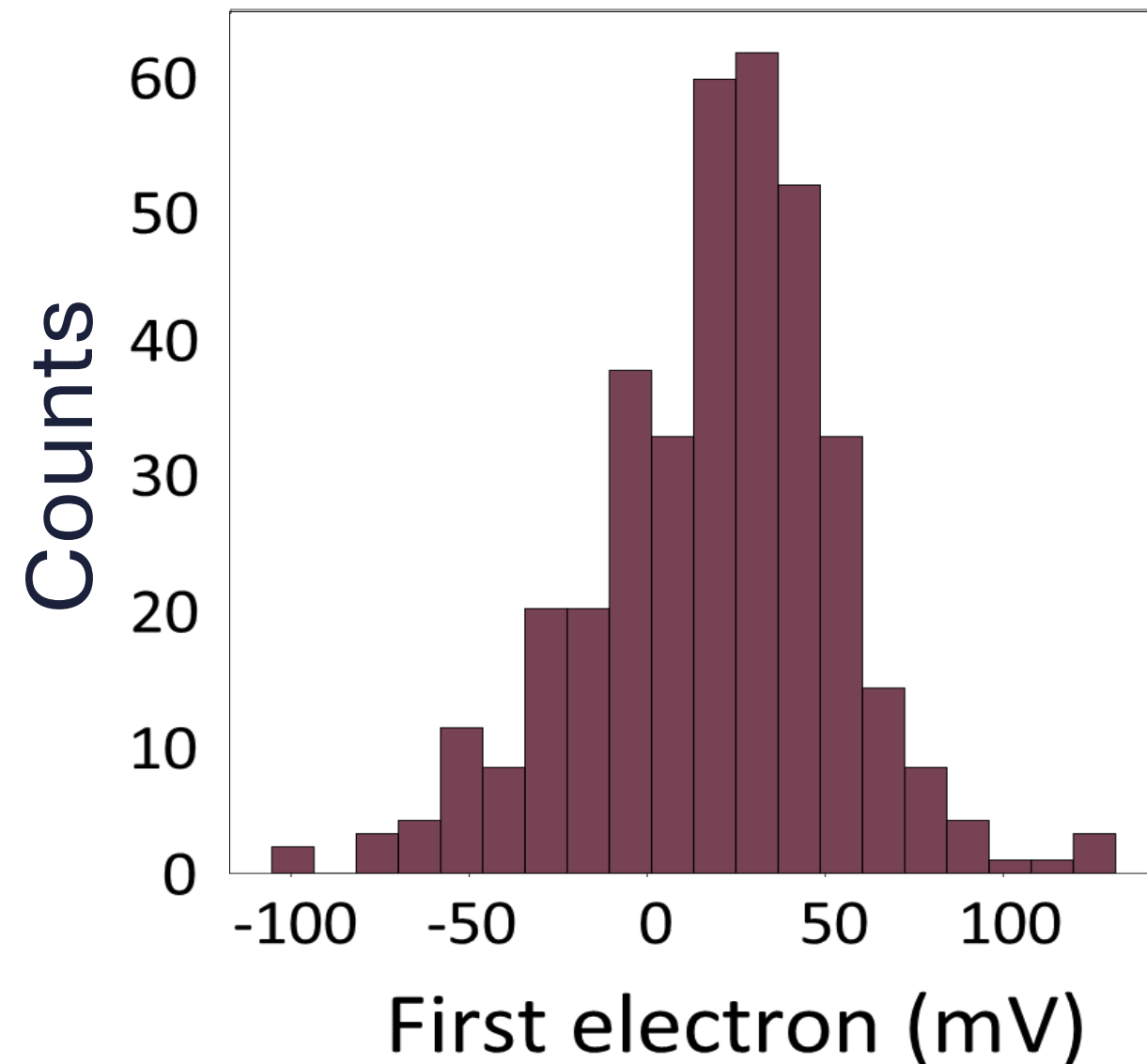


Qubit device characterization (2K): QD performance

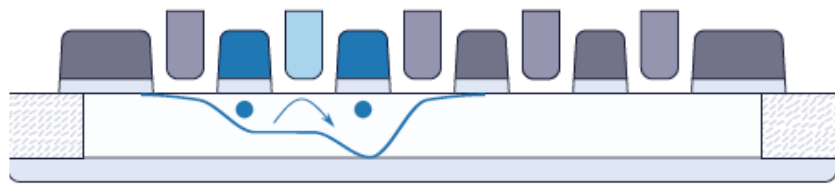
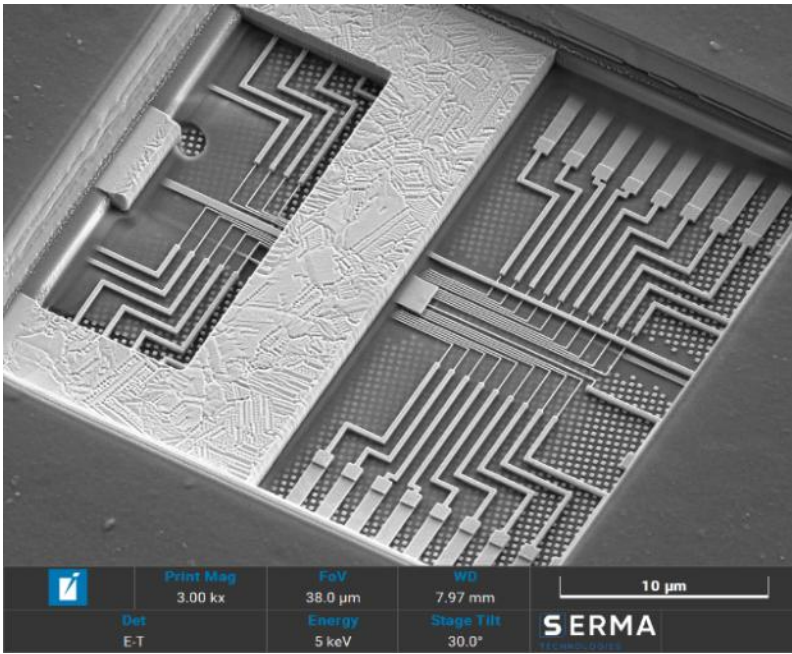
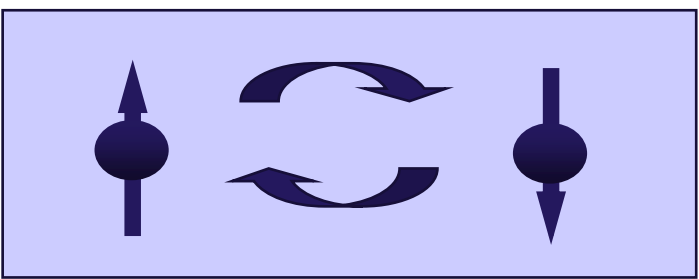
Few-electron regime with excellent variability

$$\sigma = 35\text{mV}$$

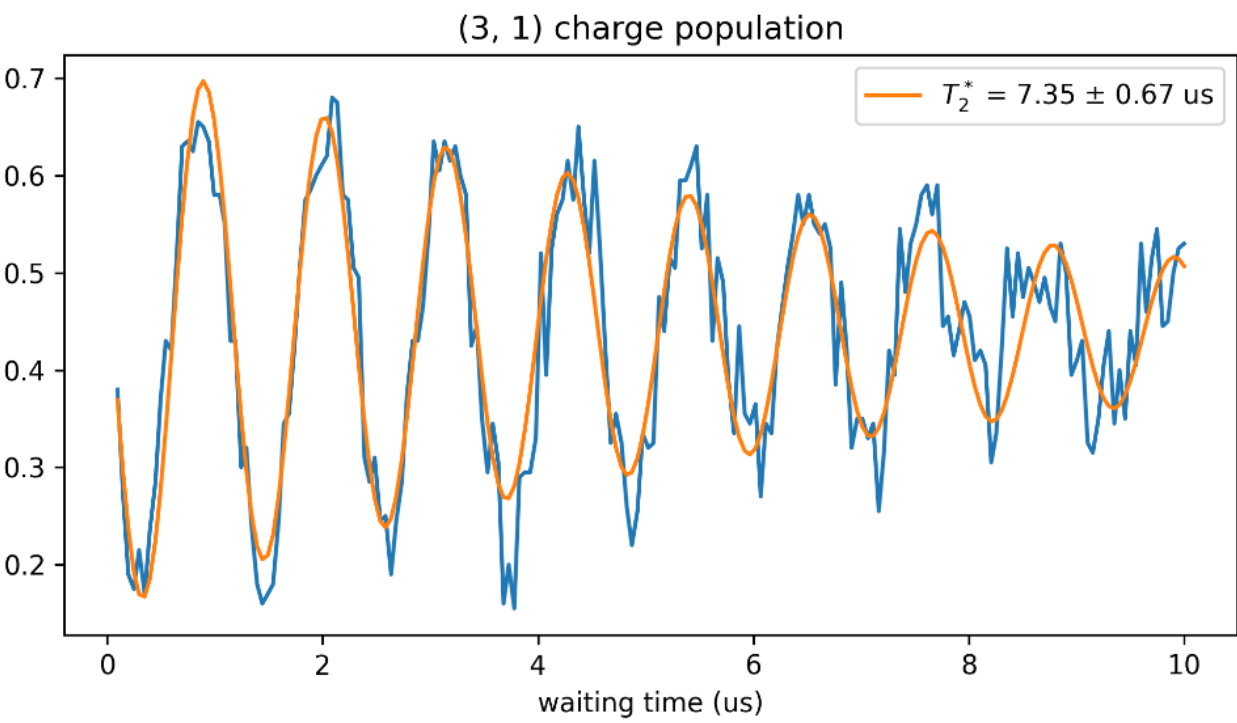
For first electron position



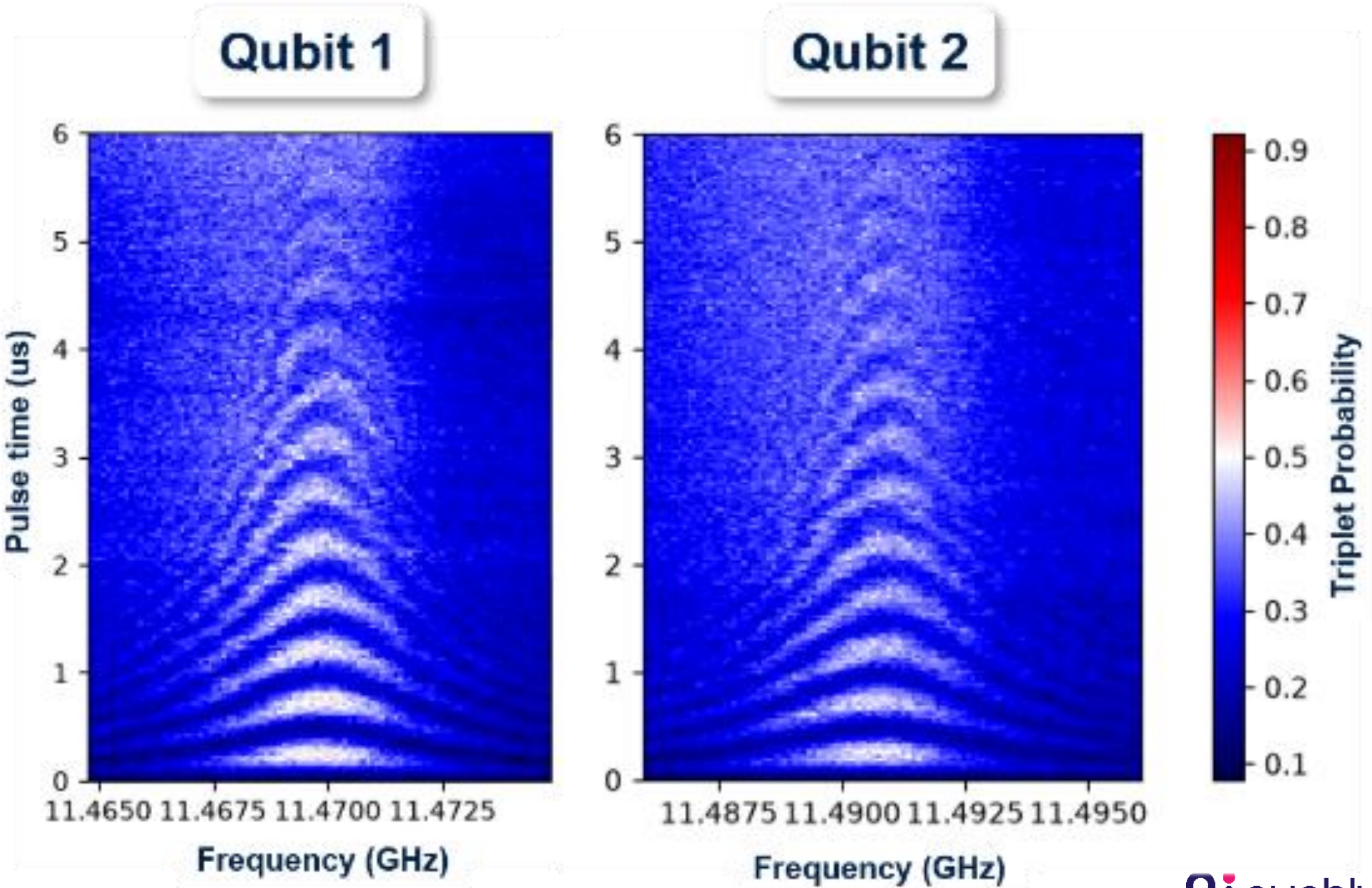
ESR manipulation and one-qubit gate in QSOI® commercial devices



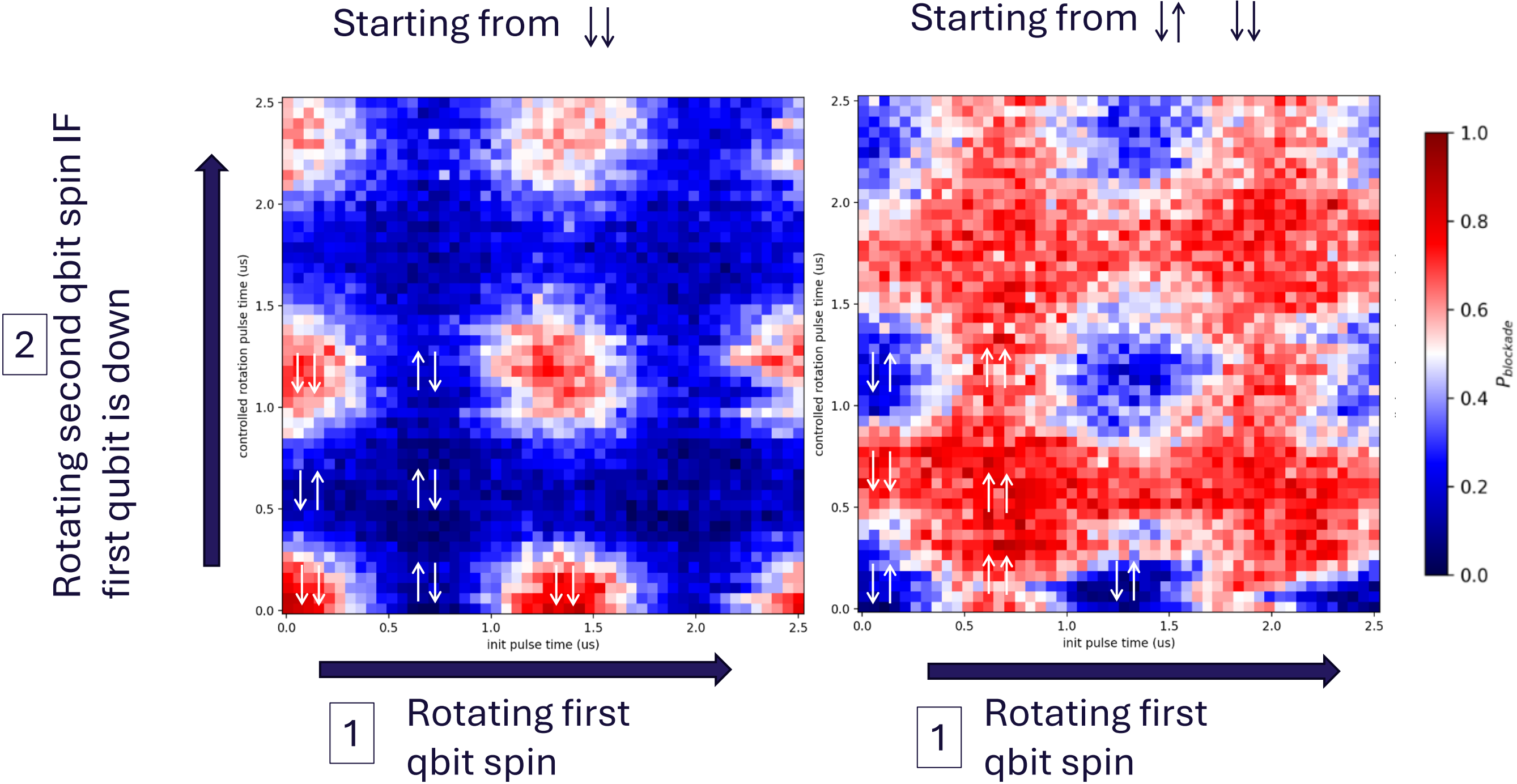
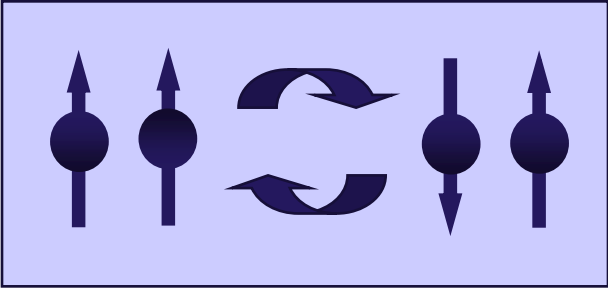
8 qubit device with ESR line



Ramsey experiments : validation of the SOITEC wafer purification



Two-qubit gate



- The spin operation on qubit 2 is conditionned by state of qubit 1

Overall Q28 Technology Development



Leveraging existing process bricks from VLSI industry for fast & reliable QuBIT development

PHASE 1: QuBIT MORPHOLOGY

Re-use existing process bricks
28FDSOI / 18FDSOI / 14FDSOI / IMAGERS

Minimize technical risks
Minimize development cycle time

PHASE 2: QuBIT STABILITY ENHANCEMENT

Re-use existing low noise technique
-eNVM & PIXEL IMAGERS

Working axes: materials, cleaning, implants

PHASE 3: QuBIT/Logic Co-INTEGRATION

Re-use existing process bricks
-28FDSOI / 18FDSOI / 14FDSOI

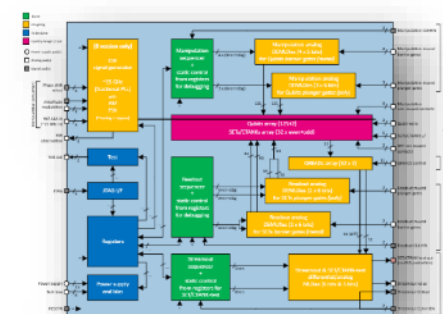
QuBIT = master / Logic= model update

PHASE 4: TOWARD 2D QUANTUM CHIP

Re-use existing process bricks
-BEOL patterning from 18FDSOI & 14FDSOI

Enabling 2-directions electrons shuttling for QEC algorithms capability

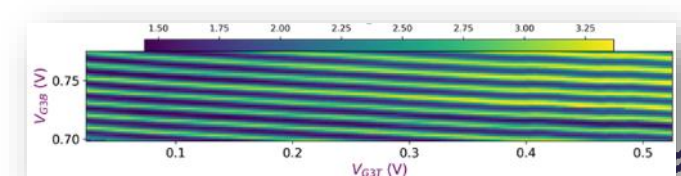
Quantum chip design



Cryostat (~100mK)



FDSOI-QuBIT Coulomb diagram



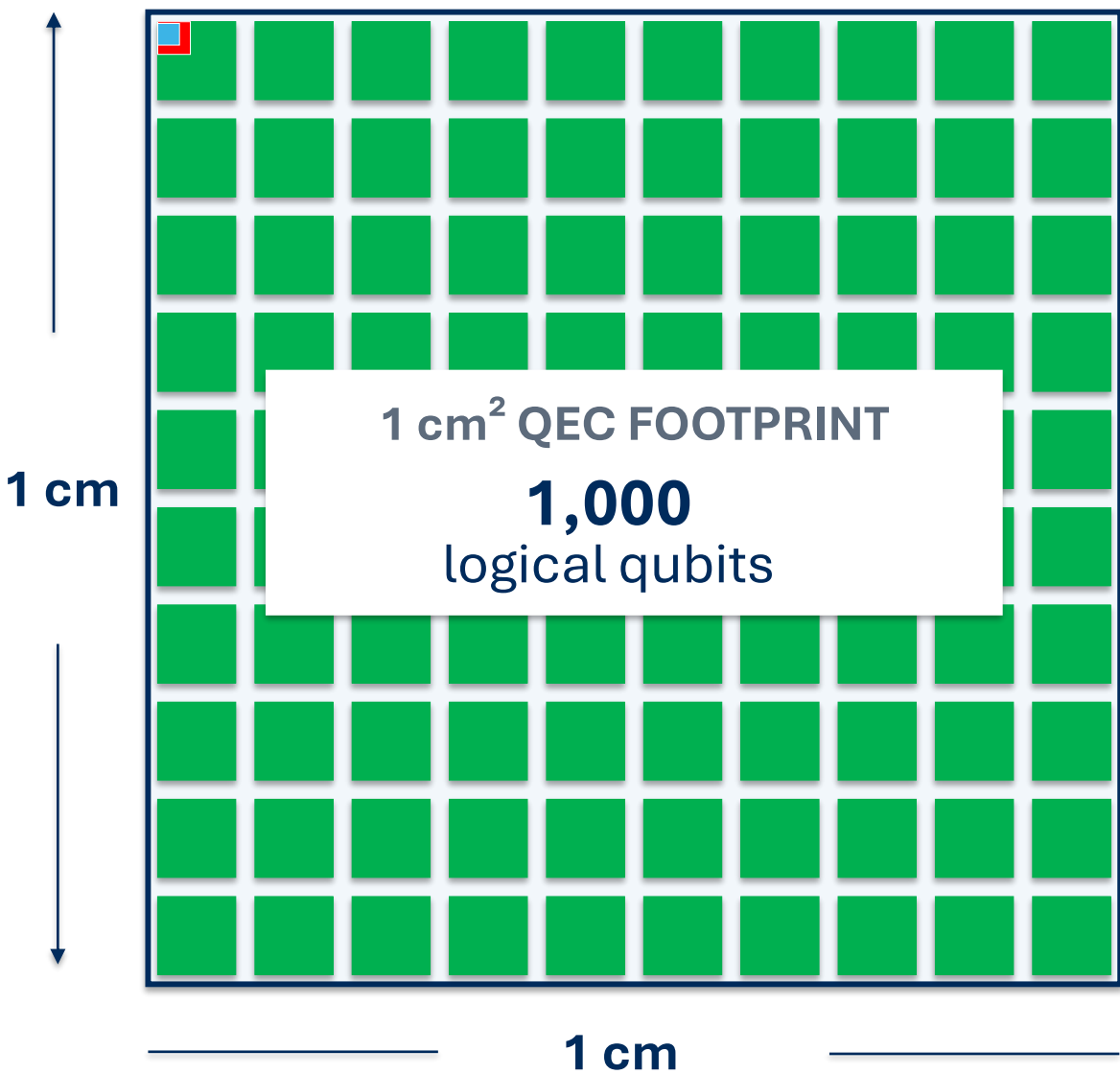
VLSI Industry Advantage | Technology Scaling



DENSITY AT THE QEC-ALGORITHM SCALE

1,000 LOGICAL QUBITS. ONE SQUARE CENTIMETER.

The entire 1 cm² footprint contains 1,000 logical qubits.



THE WHOLE FIELD

1000

Physical Qubits create 1 logical Qubit

× 1000

Logical qubits per tile

= 1,000,000

Physical qubits in 1 cm²

SCALING HIERARCHY

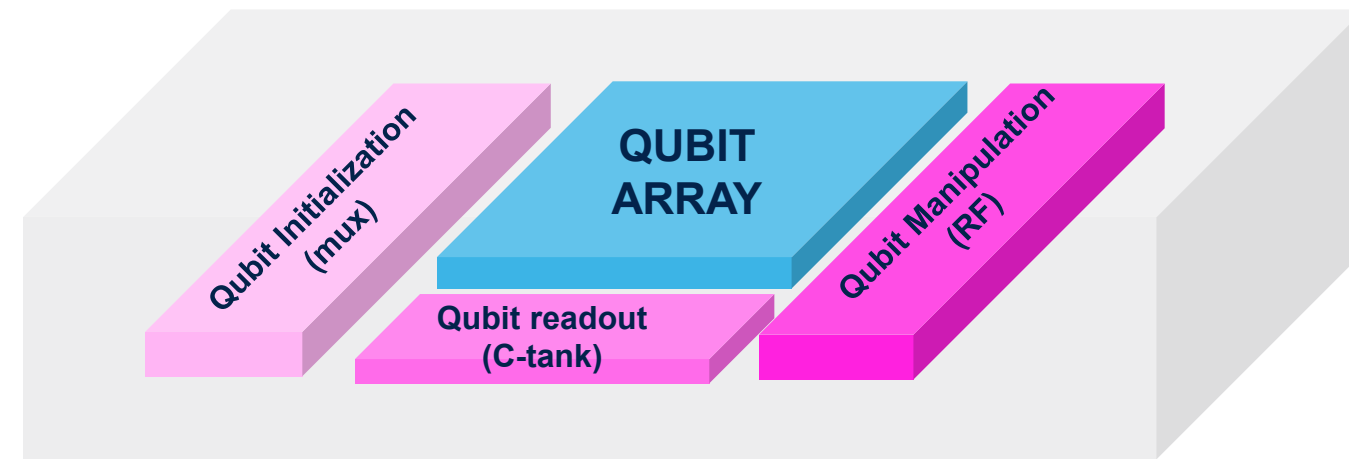
ELEMENTARY	1 qubit / SET
PHYSICAL	1 qubit + cryo-CMOS
LOGICAL	1,000 physical qubits
QEC ALGO Qubits	1,000 logical qubits

Conceptual grouping for scale communication; tile layout is not a physical floorplan.

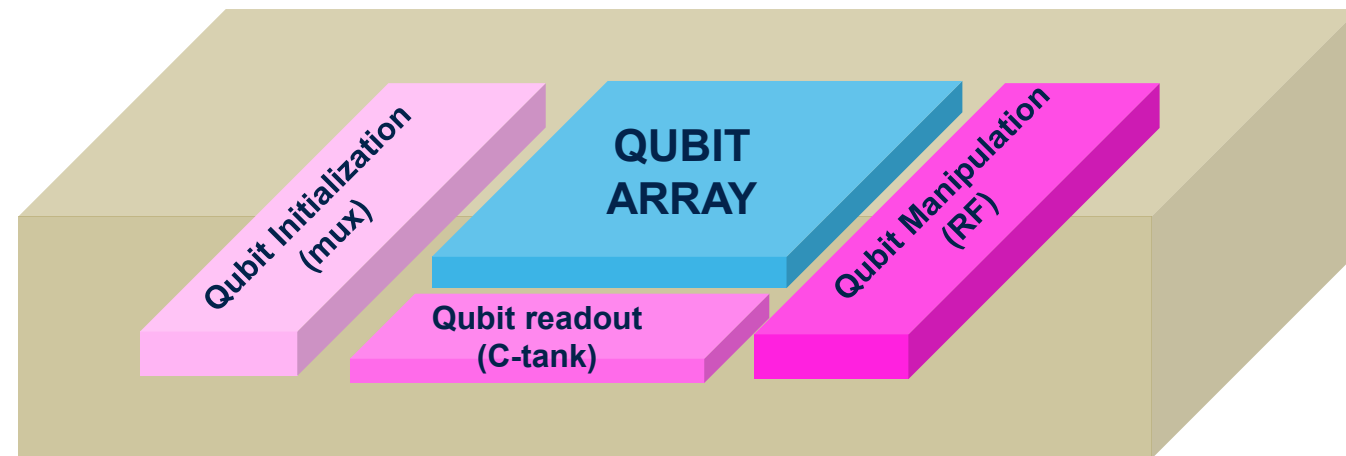
VLSI Industry Advantage | SoC Co-Integration



Quantum solution with VLSI technology



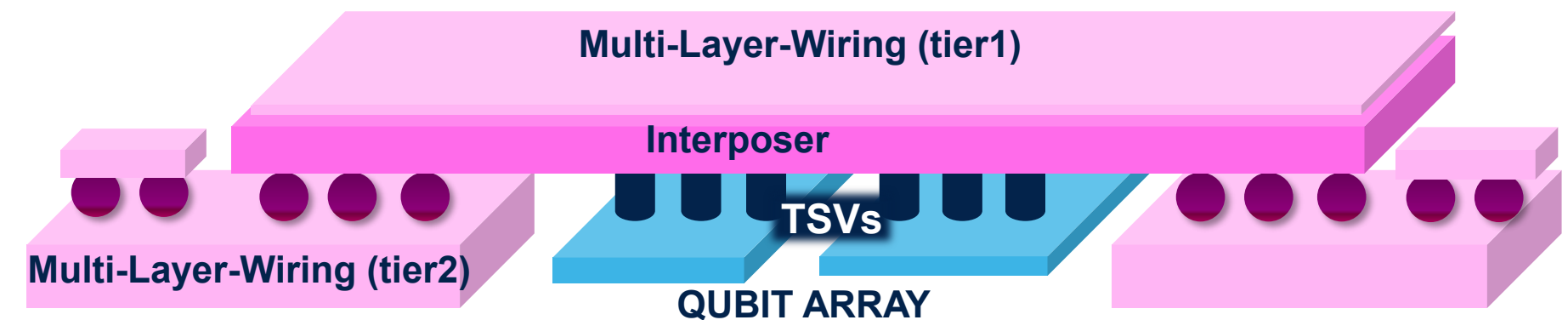
28FD-SOI technology (SoC)



28FD-SOI technology + superconducting wires (SoC)

Cryo-CMOS & qubit co-integration on same die
Leveraging aggressive design rules
Smooth path toward superconducting wires (low self-heating)

Competition (superconducting qubit or photonic)



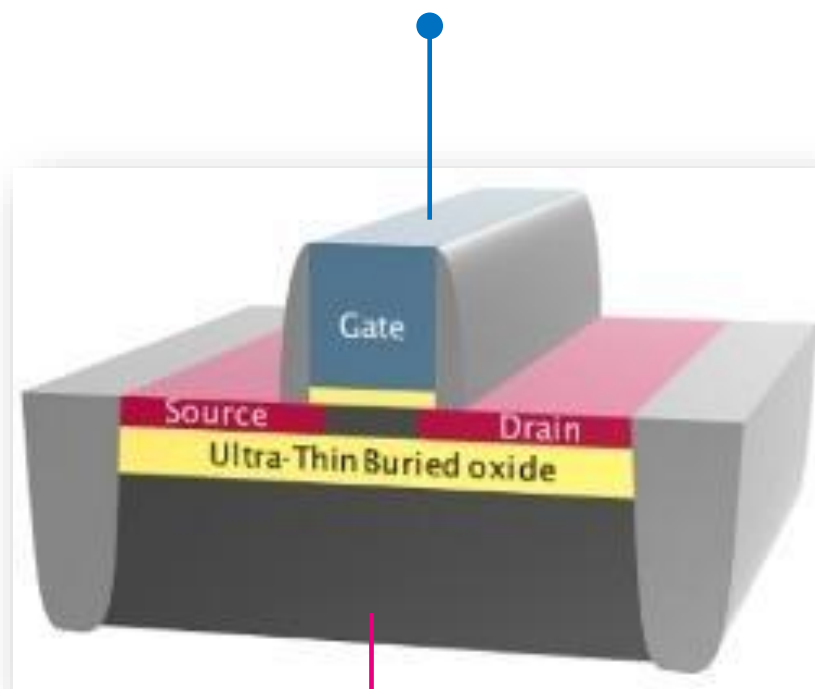
- Qubit array = native superconducting material
- Interposer → **superconductors required**
- Multi-layer wiring (tier1 & 2) → **superconducting wires required**
- TSVs → **superconductor required**
- Hybrid bonding → **with superconducting material required**

Multi-die solution → SiP with high complexity
Very big dimensions (centimeters square)
Very complex path toward superconducting wires (interposer & TSVs)

FD-SOI Transistor for Quantum Computing



Front-Gate (V_{DD})

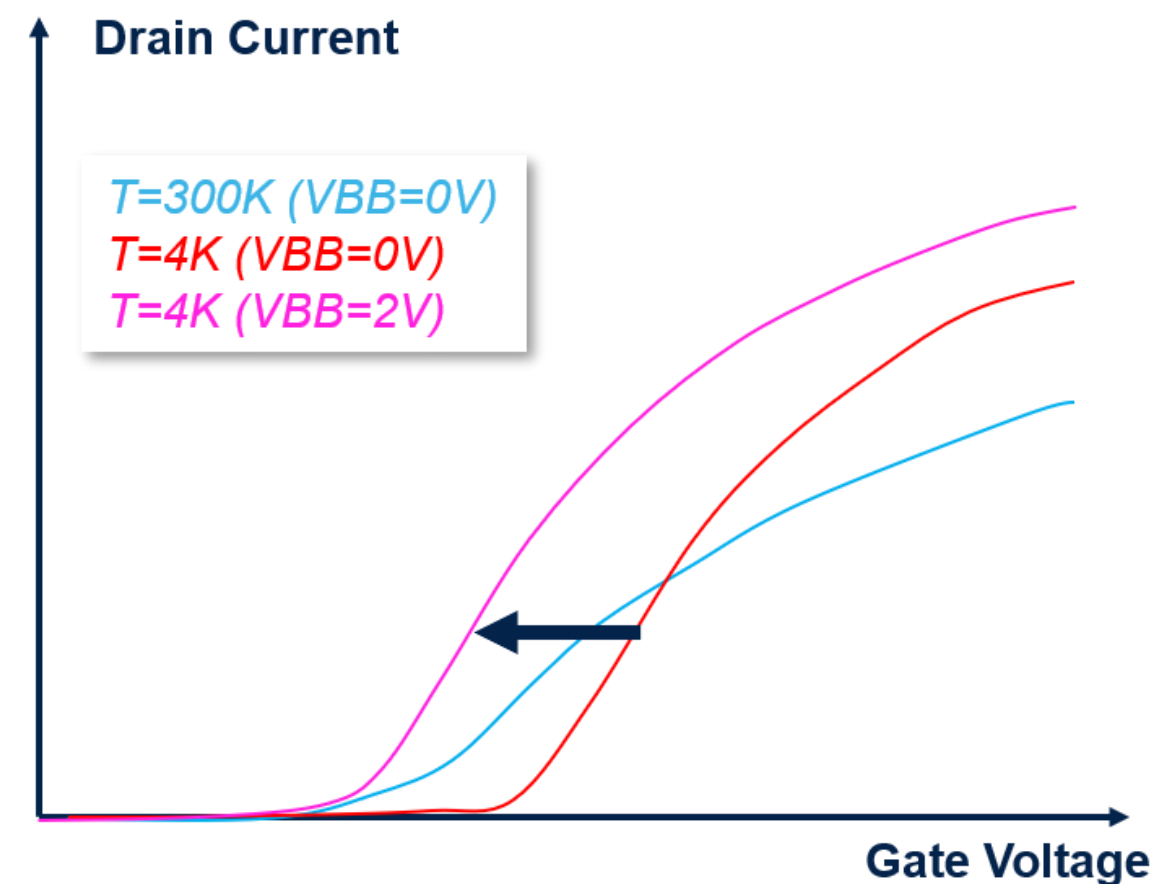


Back-Gate (V_{BB})

FD-SOI Back-gate:

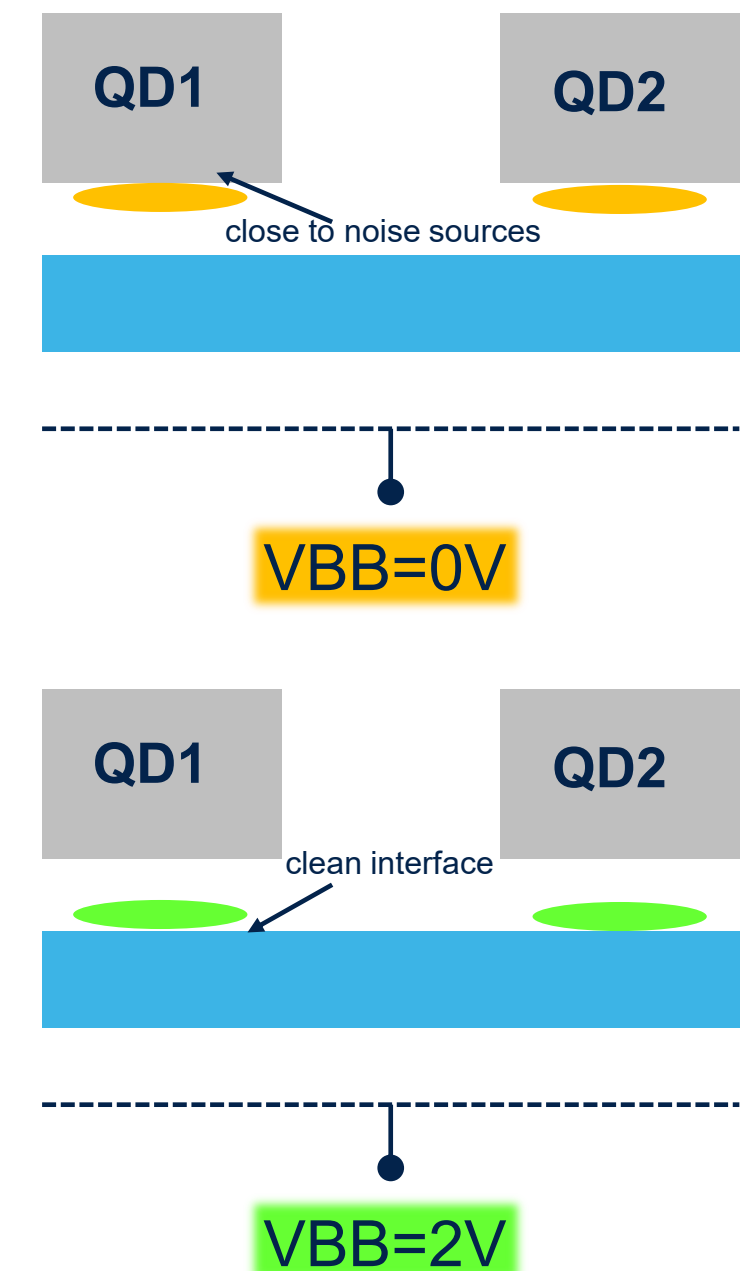
= unique knobs for further device optimization (logic and qubit)

Back gate biasing for Logic



*VT recovery with back-gate biasing
improving performance at low voltage*

Back gate biasing for qubit



*Lower charge noise in the qubit with
back-gate biasing*

System partners for an industrial product



Cryostat



Quantum error correction



Cryo-control-electronics



Measurement and Characterization



Chip design and fabrication



Wafer Production (and Purification)



Securization & PQC

Quantum algorithms



Compilation / middleware



HW/SW integration and updates

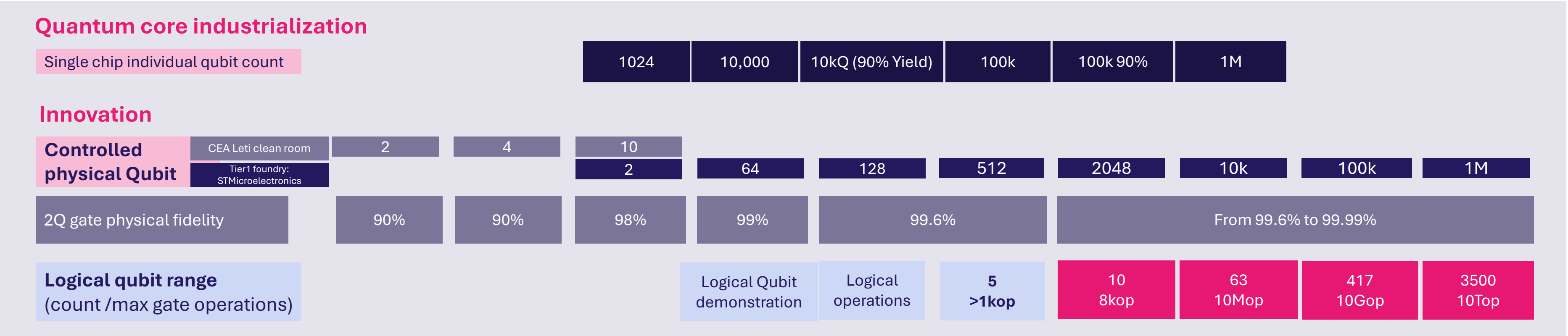
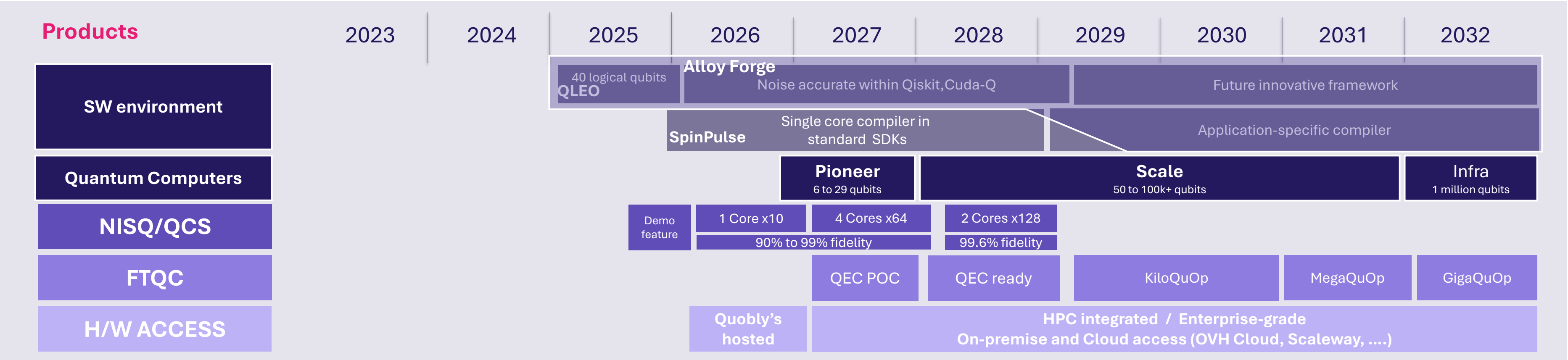
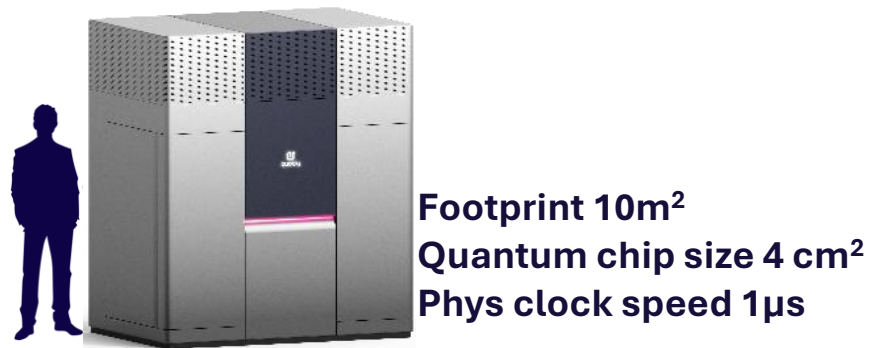
API, coms HPC

Reliability, availability, uptime

Quobly product and technology roadmap

NISQ = noisy intermediate scale quantum
QCS = quantum centric supercomputing
FTQC Fault-tolerant quantum computing

QEC = quantum error correction
QSDK = quantum SDK eg QisKit, bracket,...



Quantum is already on chip

- Quantum is becoming an engineering problem
- Using semiconductor strengths is an elegant way to solve it
- ST and Quobly are developing this quantum technology: QSOI®

1 million qubits. Built for deployment. Built for operation. Built for scale.