

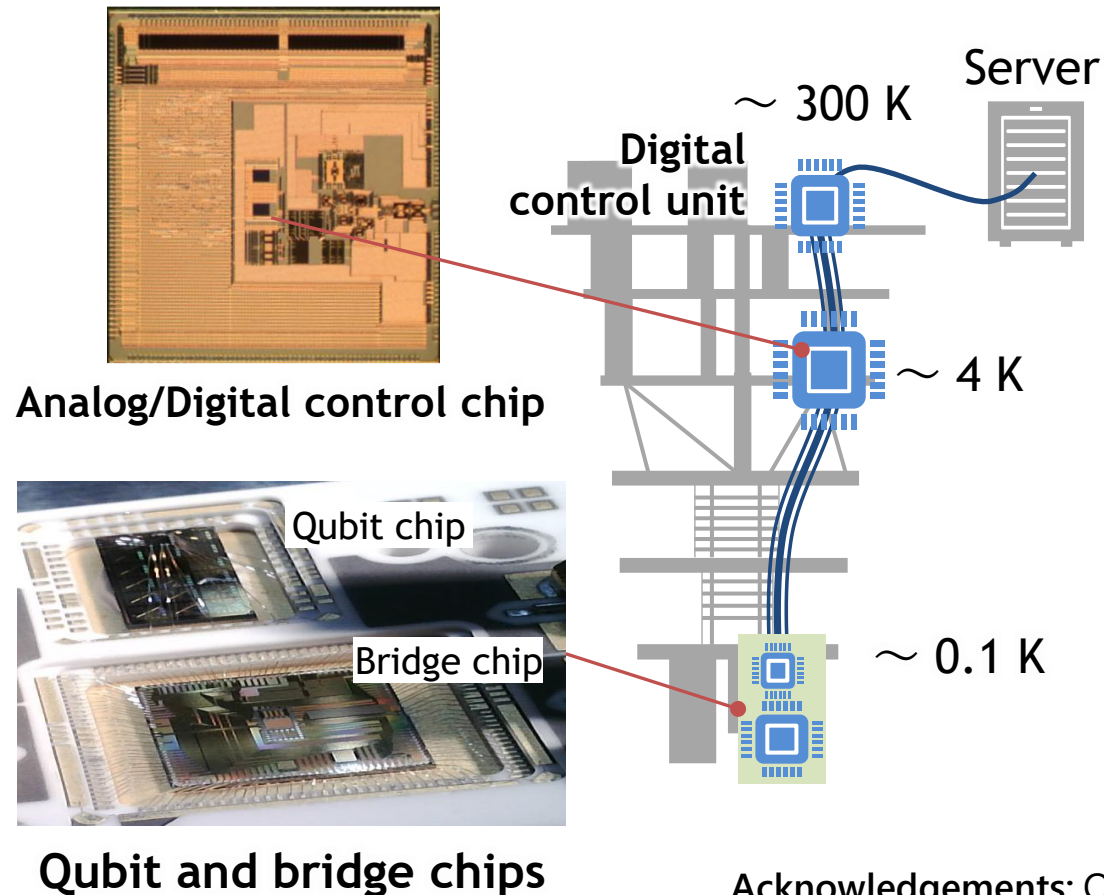
Semiconductor Industry Advancing Quantum meeting, 23rd September 2026
Institut Imagine, Paris

Technology development for large-scale Silicon quantum computer

Tomonori Sekiguchi
R&D group, Hitachi Ltd.

Project structure

- We are developing **computer system** based on the results of **fundamental research** of high-fidelity qubit operations in collaboration with academia.
- **Advanced technologies** such as cryo-CMOS chip and packaging are also developed for large-scale integration of qubits that will bring breakthroughs to the system.

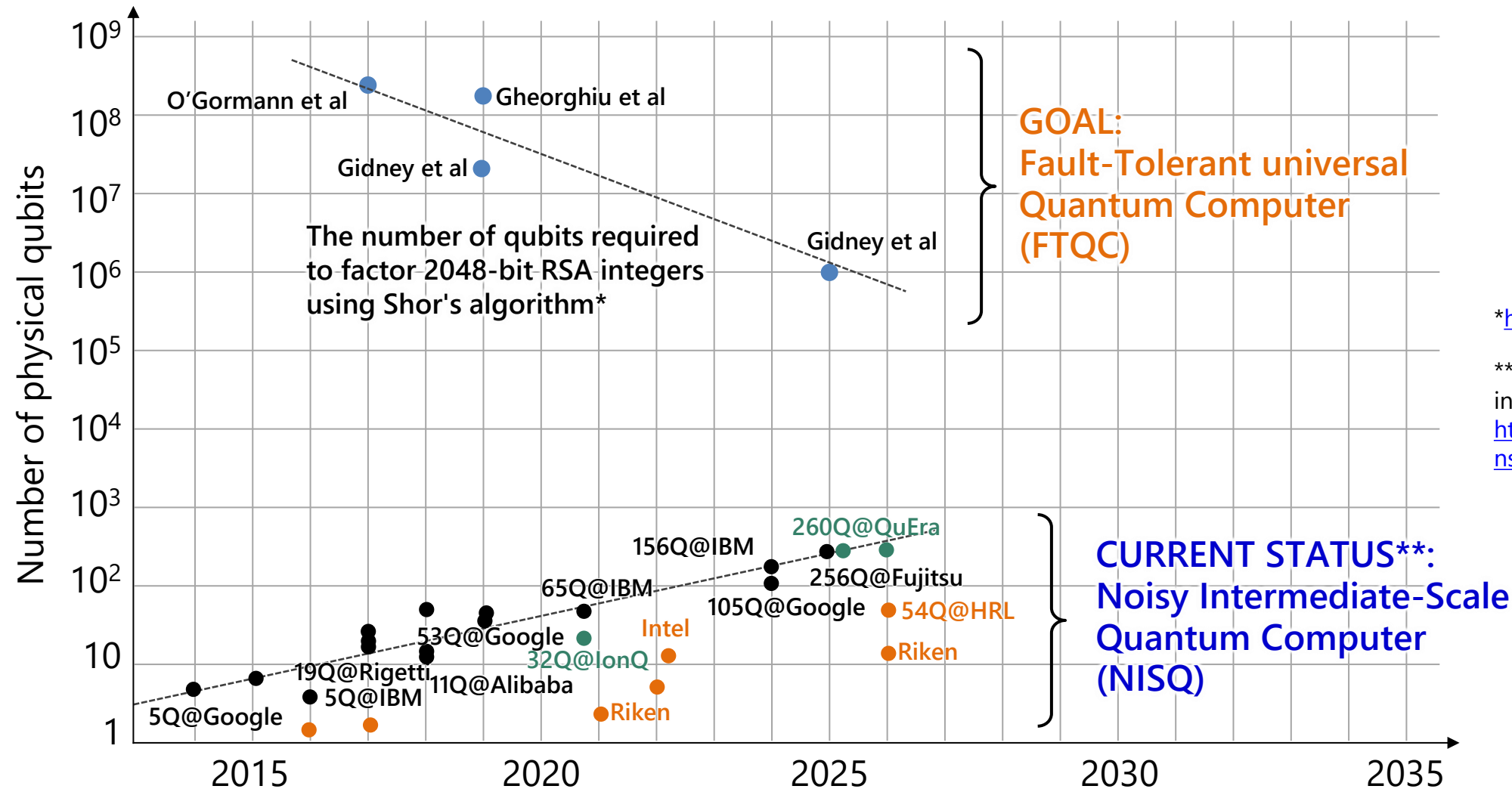


R&D theme		
1	Quantum Computing System Architecture	Hitachi
2	Cryo-electronics	Hitachi, Kobe University
3	Qubit operation	RIKEN, University Tokyo, Science Tokyo
4	Device Fabrication	imec

Acknowledgements: Quantum computing development is supported by JST Grant No. JPMJMS2065.

Goal and challenges

- Silicon-qubit has potential advantage of integration process, but the current integration level is behind.
- It is necessary to achieve **large-scale integration** and to implement **efficient error correction (QEC) codes**.



*<https://arxiv.org/abs/2505.15917>

**Created based on the following information:
<https://www8.cao.go.jp/cstp/moonshot/concept6.pdf>

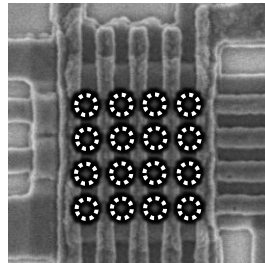
Space constraints for QEC code implementation

● Qubit integration architecture

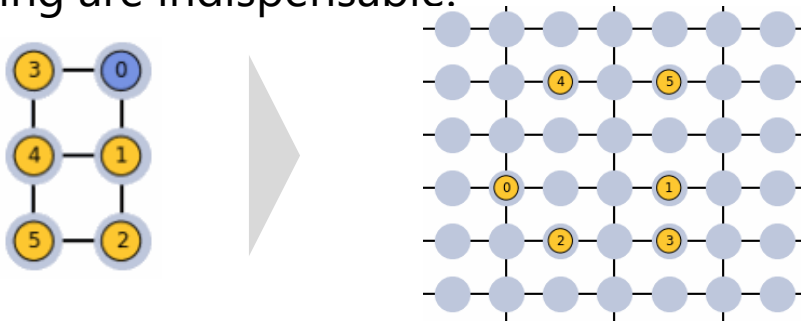
- ✓ The dense 2D array structure is used in semiconductor memory.

Issues:

- (1) Only qubits close to the edge can be read-out.
- (2) Qubits cannot be controlled independently.



- ✓ A sparse qubit layout and qubit shuttling are indispensable.



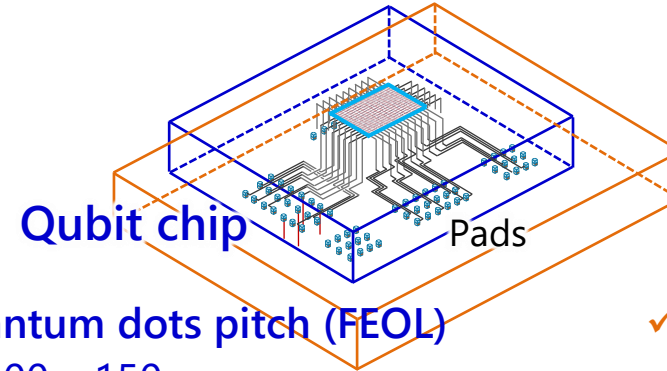
Conventional qubits

$$(N_{\text{quantum dots}} = N_{\text{qubits}})$$

Shuttling qubits

$$(N_{\text{quantum dots}} \gg N_{\text{qubits}})$$

● Fanout of wiring from the qubits



✓ Quantum dots pitch (FEOL)

- 100 – 150 nm
Array: 150 x 150 μm^2 [1M qubits]

✓ Metal Layer pitch (BEOL)

- 20 - 30 nm (3 – 4 nm Node)

✓ Pad pitch (3D integration)

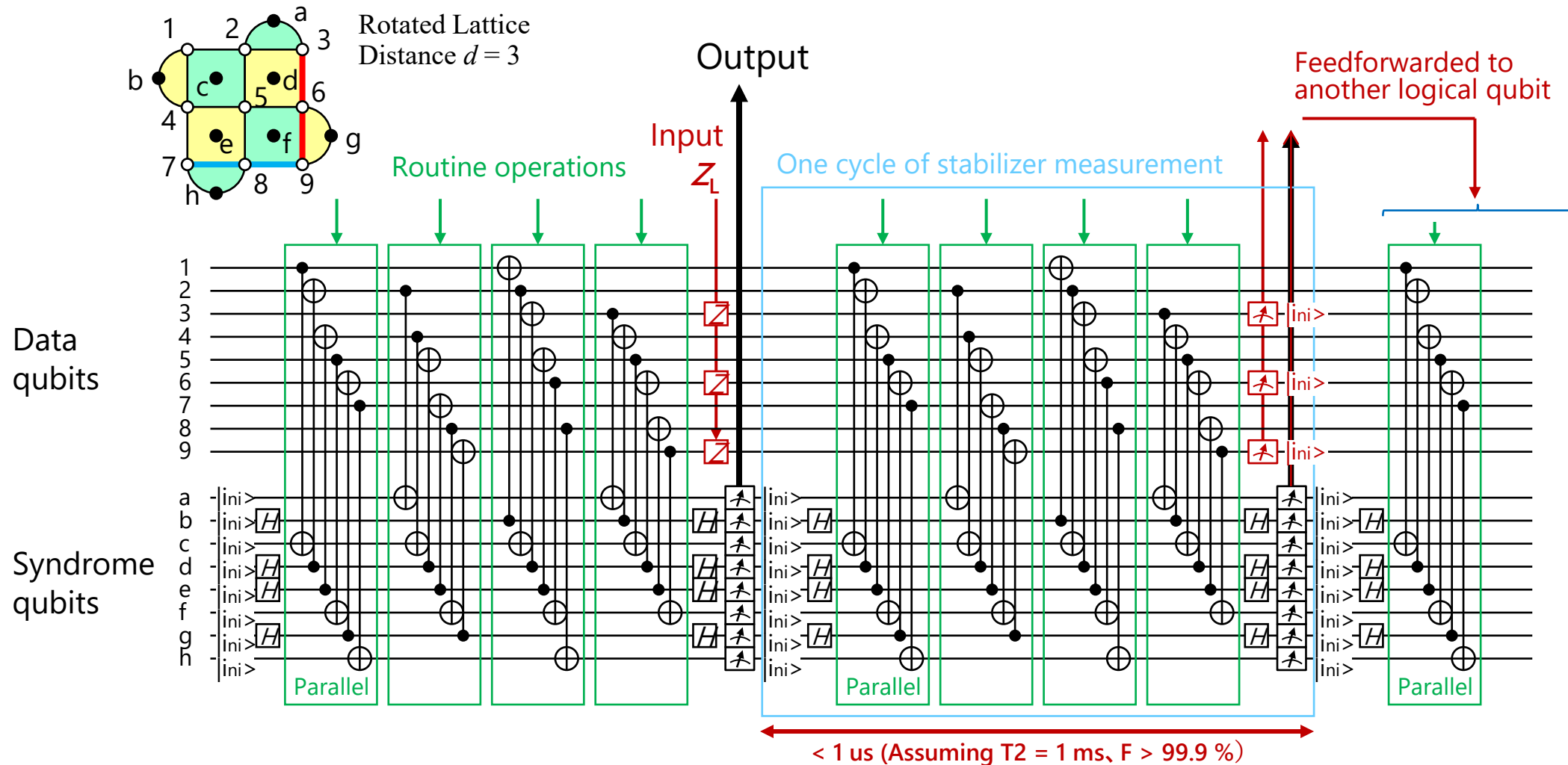
- 20 μm (Die Stacking, μbump)
 $\Rightarrow$ 250k pads* [1,000+ qubits]
- 1 μm (Wafer-to-Wafer Hybrid Bonding)
 $\Rightarrow$ 100M pads* [100k–1M qubits]

- ✓ Since it is not practical to route tens of thousands of wires inside a fridge, integration of **MUX/DEMUX circuits** is essential.

*Assumed a qubit chip size of 10x10 mm^2 .

Time constraints for QEC code implementation

- It is necessary to execute the QEC processing within the time constraints.

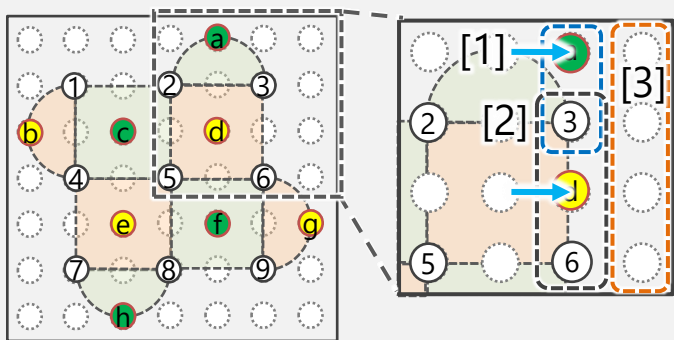


Qubit integration for quantum error correction (QEC)

- A scalable solution is required for both the number of physical qubits and the surface code distance.

2D Dense Matrix Layout

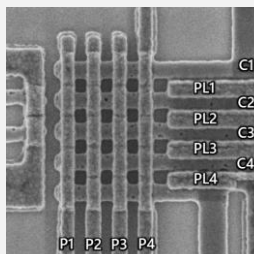
- Mapped surface code on a 2D array



[1] Shuttling, [2] CNOT, [3] Readout

✓ Scalability

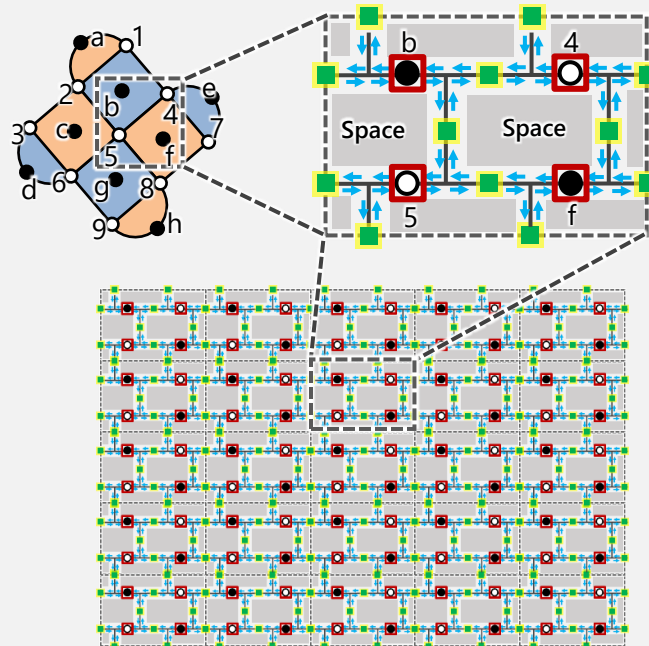
✗ Unable to fanout
the control wiring



2D array (4 x 4)

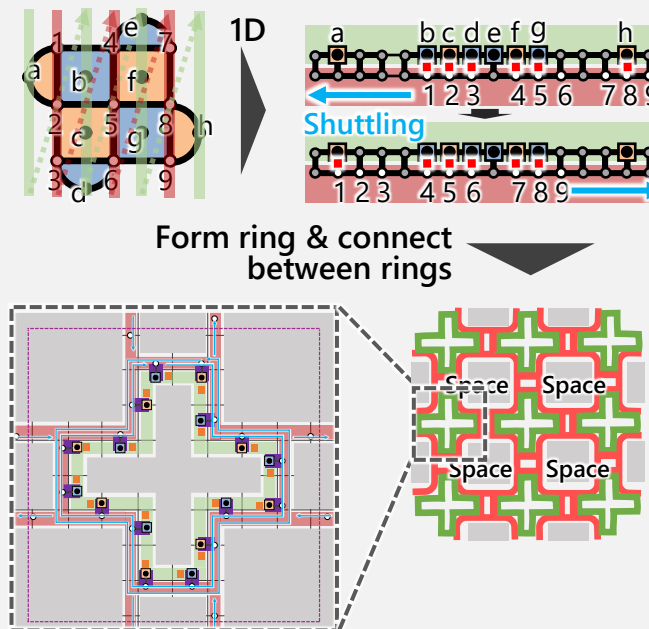
2D Sparse Layout

- Mapped surface code on Brick-patterned 2D sparse layout



Quasi-2D Sparse Layout

- Converts surface code to a 1D format & creates a quasi-2D structure



Dense

Wiring density

Sparse

Easy

Scale-up

Difficult

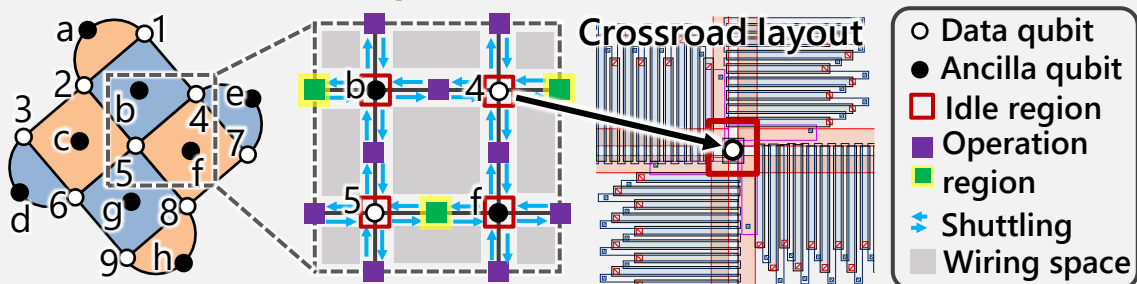
Brick-patterned 2D sparse layout

- Designed a brick-patterned 2D sparse layout that effectively relaxes the shuttle speed.

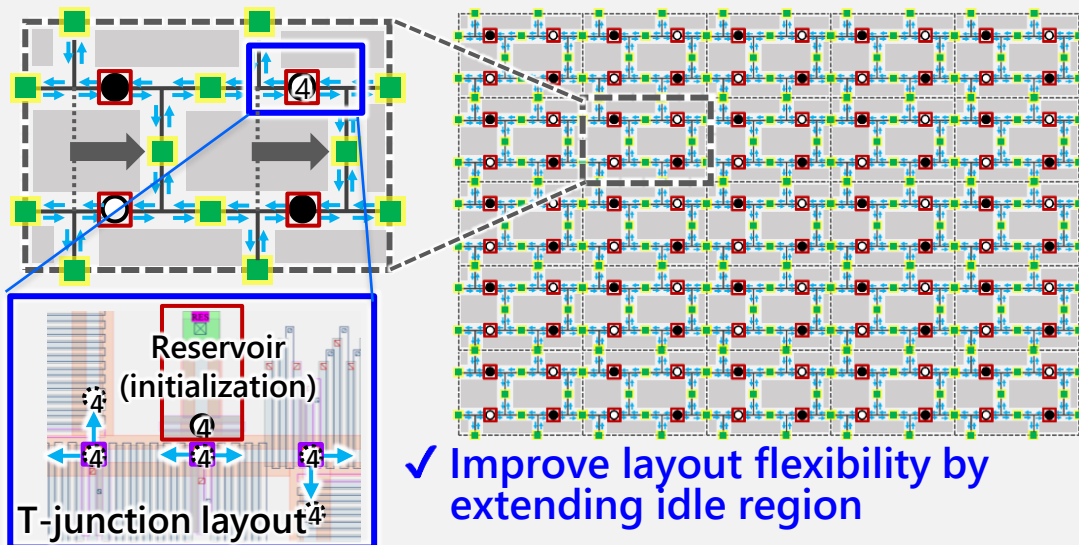
Brick-patterned 2D sparse layout

Conventional: Spiderweb*

*UT Delft, PRApplied 18, 024053

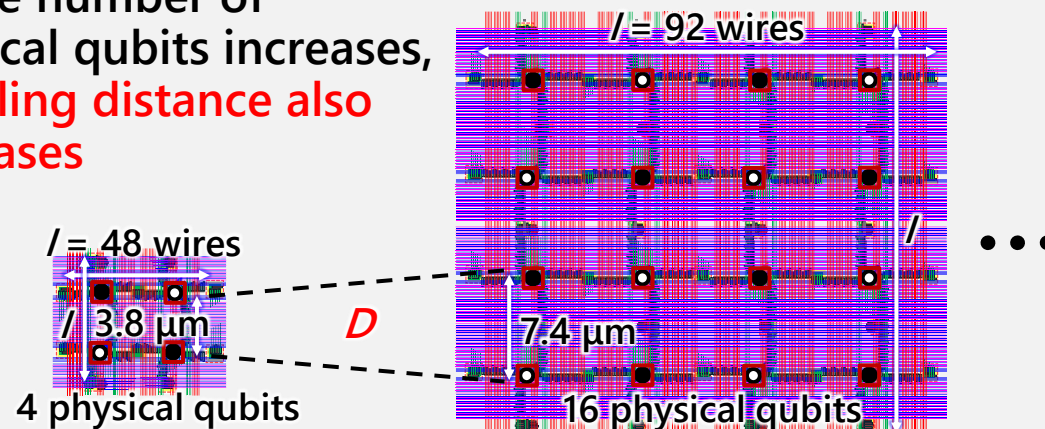


Proposed: Brick-patterned 2D Sparse Layout



Required Shuttling Speed

- As the number of physical qubits increases, **shuttling distance also increases**



Assumed: 40nm pitch, 4-layer metal wiring process

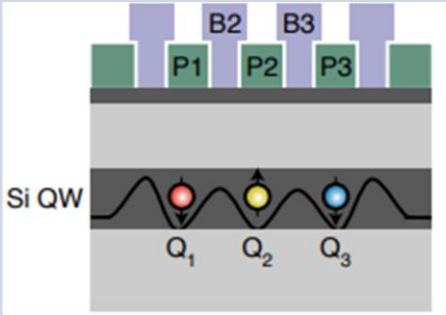
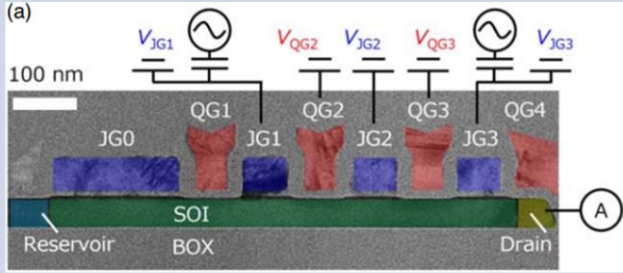
Physical qubits	Num. of routing wires $2l$ (units)	Spatial width D (μm)	Shuttling speed (m/s)
16	184	7.4	9
64	360	14	18
256	712	29	36
1024	1416	57	71

✓ Scalability regarding code distance

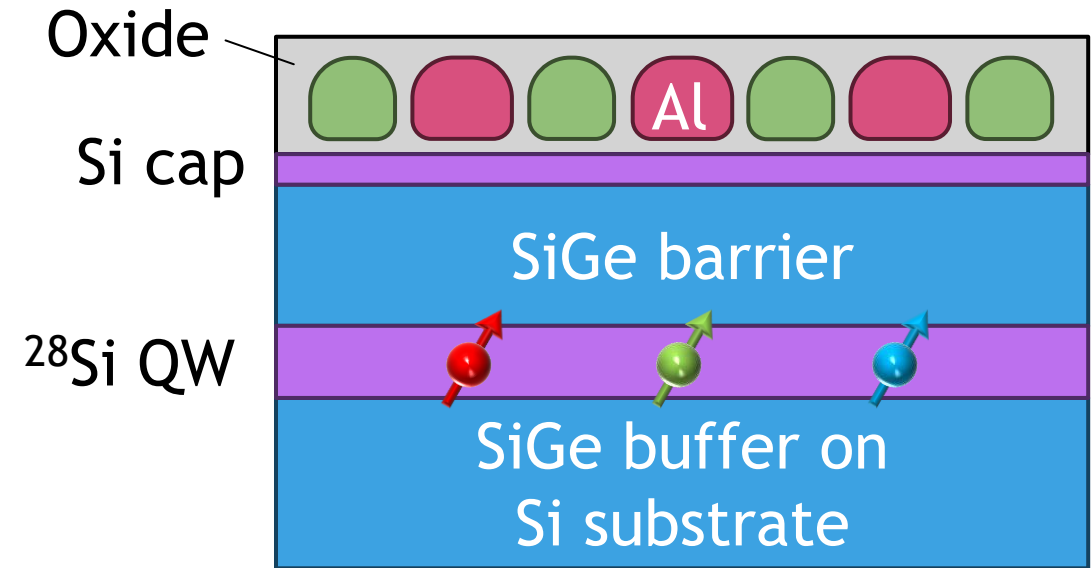
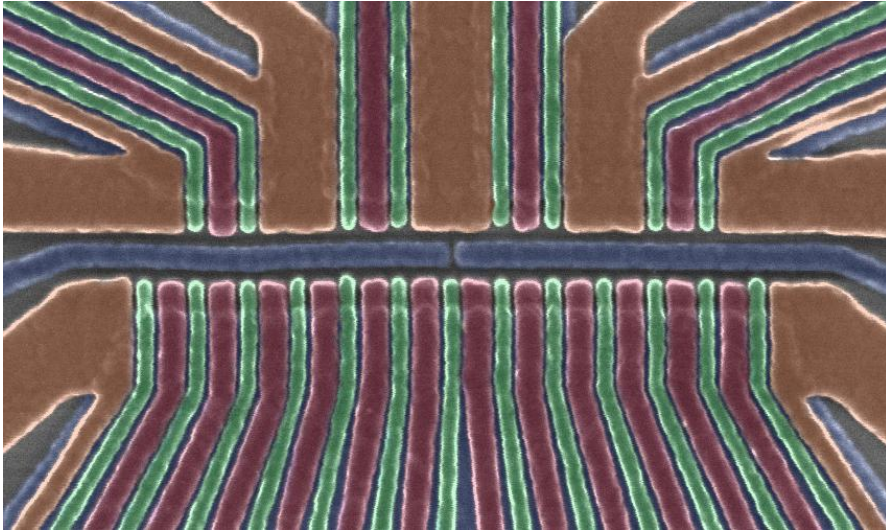
✗ Shuttling speed demands increase with scaling

Options for silicon-spin qubits

- Developing multiple device prototypes in parallel.

	Si/SiGe (RIKEN)	Si-MOS (Hitachi)	Concerns
Device structure			
Confinement structure (Perpendicular direction)	Well structure: SiGe 30nm / Si 8nm / SiGe 30nm	Well structure: SiO₂ 5nm / SOI 50nm / BOX 145nm or bulk	- Charge in the gate - Valley degeneracy/splitting
	Gate material: Al/Al₂O₃	Gate material: Poly-Si/SiO₂	
Confinement structure (In-plane direction)	Si - SiGe surface	SiO₂ - Si surface	Surface roughness
	Isolation: Field isolation	Isolation: STI or Field isolation	Fixed charges

12 qubit device fabricated in RIKEN

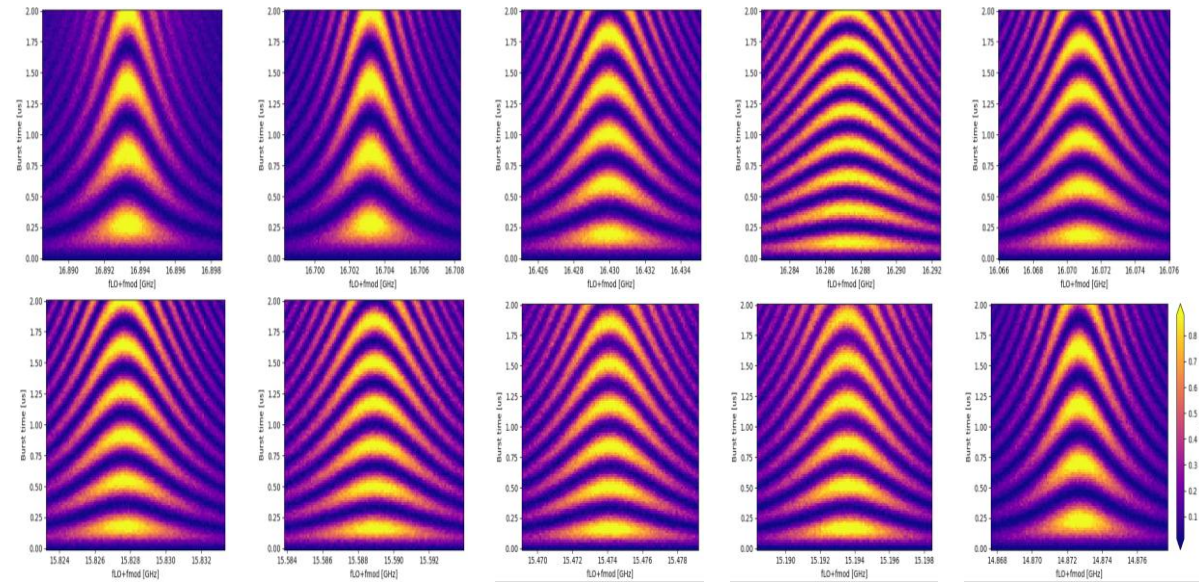
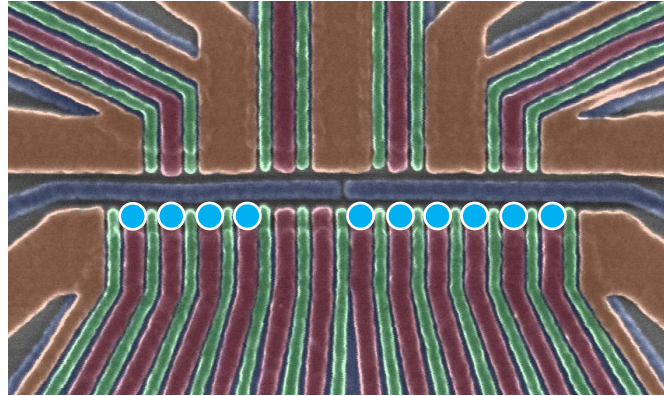


Heterostructure Si quantum well for less disorder and charge noise

Isotope purification of ^{28}Si to deplete nuclear spin-carrying ^{29}Si (4.7% in $^{\text{nat}}\text{Si}$)

Thin Al_2O_3 oxide for lower defect sites

Characterization of 10 spin qubits (Si/SiGe)

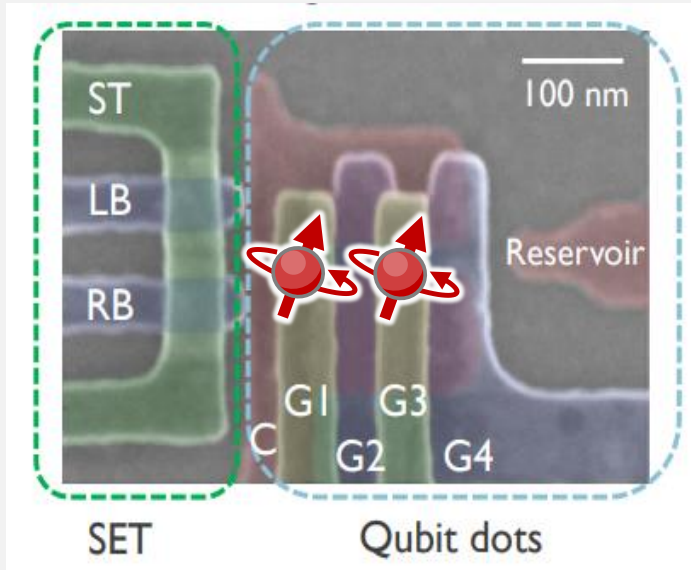


	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10
Ramsey T_2^* (μ s)	3.5	2.7	5.4	6.9	4.5	5.3	4.0	4.8	3.2	4.1
Hahn echo T_2^H (μ s)	42	105	76	115	93	65	109	111	82	67
Valley splitting E_V (μ eV)	640	600	648	504	470	280	320	120	170	400

Control fidelity >99.9%
is consistently obtained

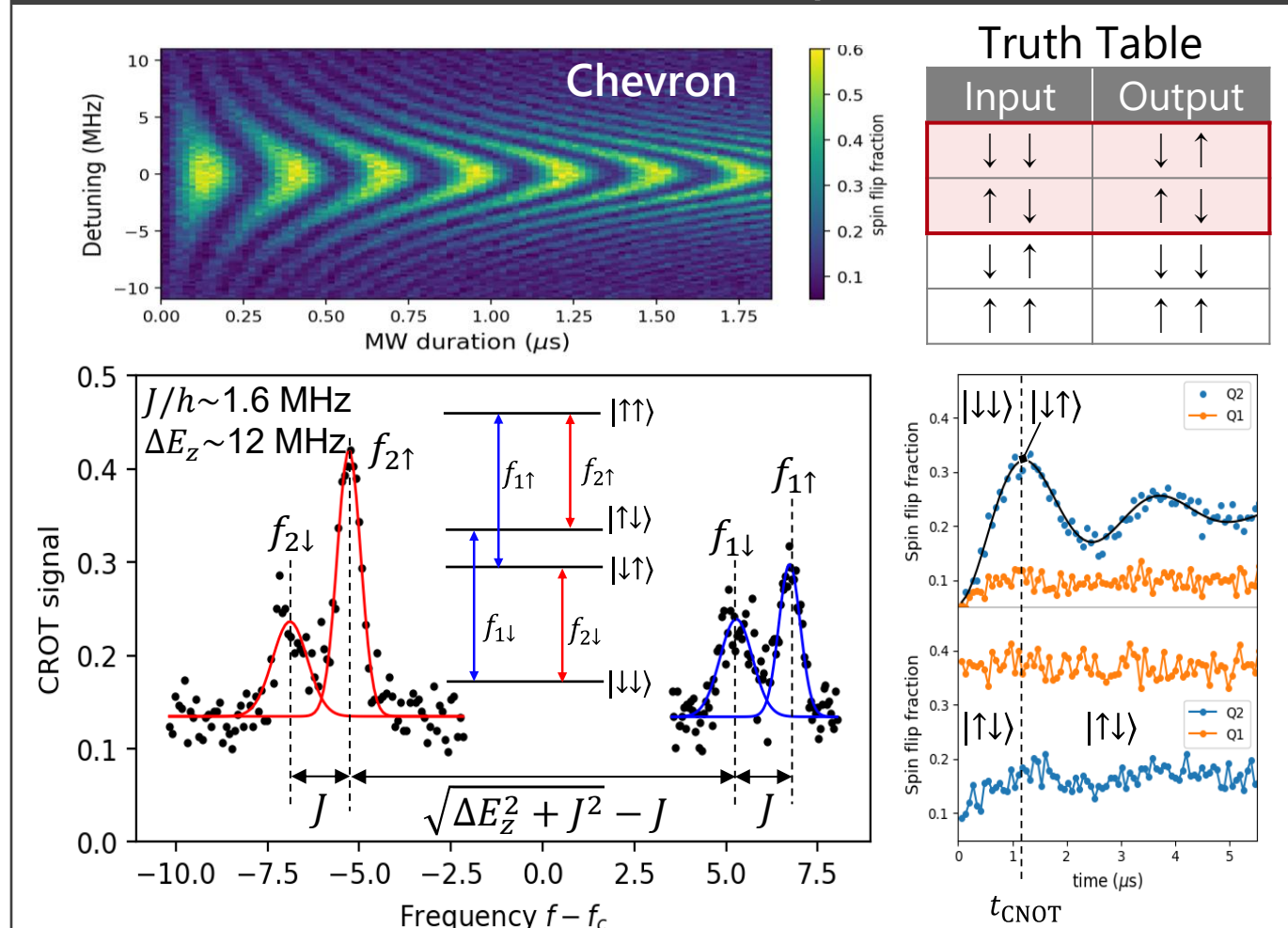
Two-qubit operations in Si-MOS qubits

- Established a cooperative relationship with imec.
- Instead of STI, field isolation is used to make the quantum dot structure less noisy.



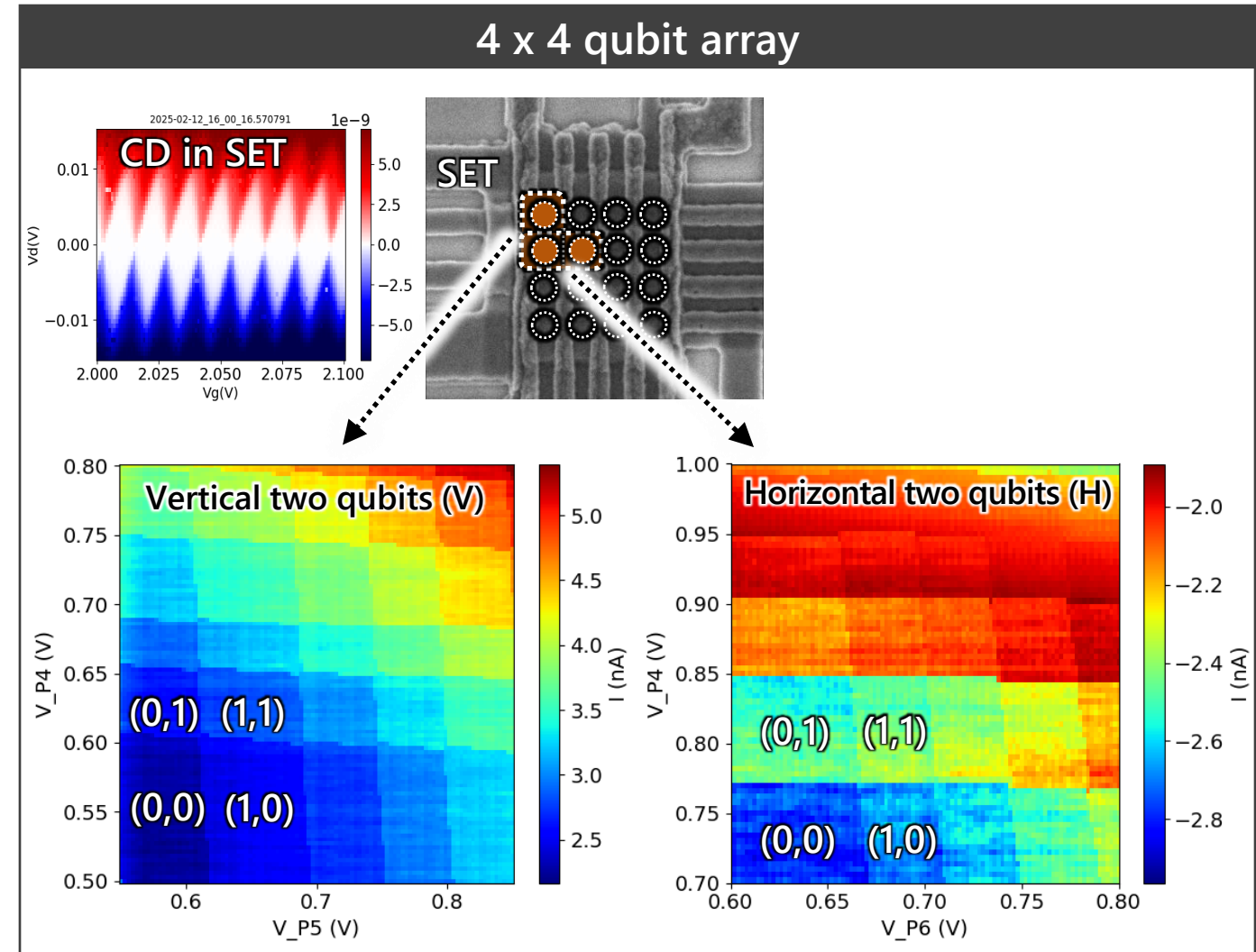
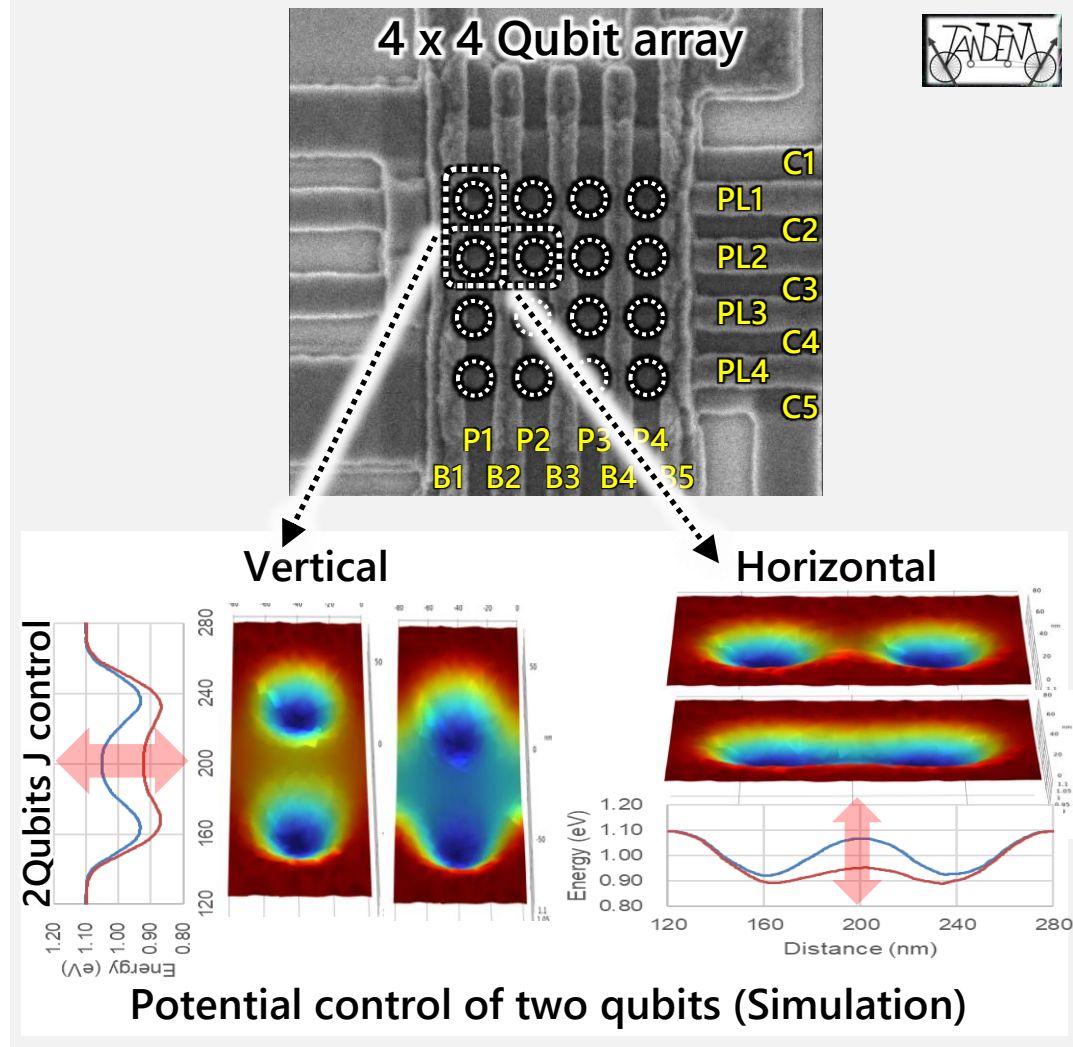
T. Kuno et al., Quantum Innovation 2025

2 Qubit control (CROT Operation)

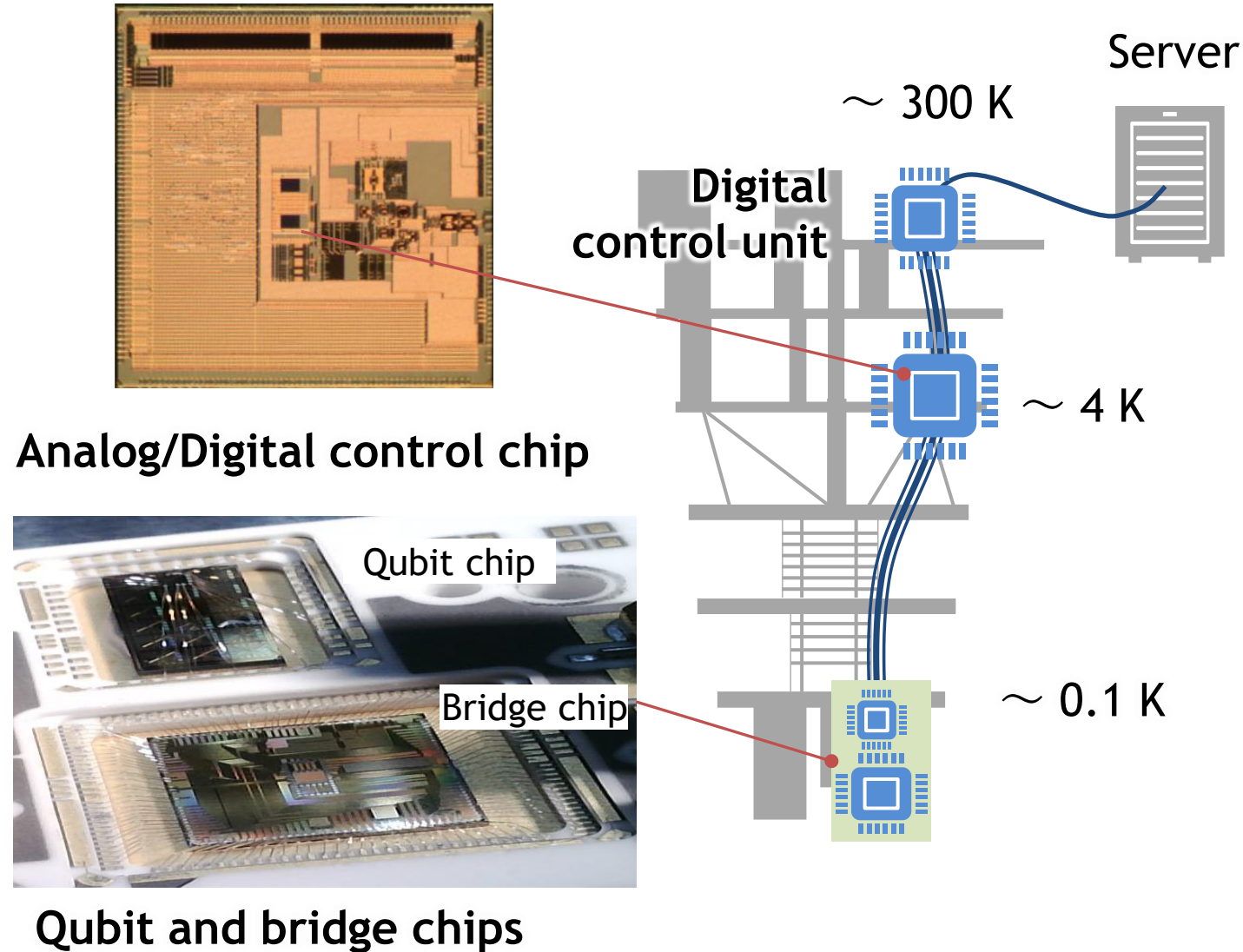


4x4 Si-MOS qubits

- Prototyped 4x4 qubit array toward large-scale arrays
- Confirmed J coupling can be controlled in two qubits in each of the vertical and horizontal directions



Hierarchical architecture with cryo-electronics

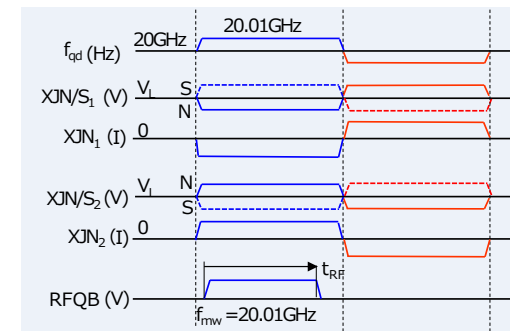


```
blk.add(EXE(0, RFC(2, 100, 1.0, 1.0, 'P')))  
blk.add(EXE(0, SWC(0)))  
blk.add(EXE(0, BVS(['XJN1', 'VL2n'], ['YJW0', 'VL3w'])))  
blk.add(EXE(0, BVS(['XJS1', 'VL1s'], ['YJE0', 'VL4e'])))  
blk.add(EXE(0, BVS(['XJN2', 'VL1n'], ['YJW1', 'VL4w'])))  
blk.add(EXE(0, BVS(['XJS2', 'VL2s'], ['YJE1', 'VL3e'])))  
sequence.add(blk)  
blk = Block()  
blk.add(EXE(0, BVS(['XJN1', 'VL1n'], ['YJW0', 'VL4w'], SWT(1), RFT(1))))  
blk.add(EXE(0, BVS(['XJS1', 'VL2s'], ['YJE0', 'VL3e'])))  
blk.add(EXE(0, BVS(['XJN2', 'VL2n'], ['YJW1', 'VL3w'])))  
blk.add(EXE(0, BVS(['XJS2', 'VL1s'], ['YJE1', 'VL4e'])))  
sequence.add(blk)
```

Control Sequence

```
0 00000000000001000000000000000101000111101000000000101000111101  
1 00000000000001000000000011000010100011110100010000001111010111000  
2 00000000000001000000000011100101000111101010010010011001100110011  
3 00000000000001000000000101000111101011100000011000100011110101110  
4 000000000000010000000001011010100011110101100110101110000101000  
5 00000000000101100000000000000000000100000101000000000010000100  
6 000000000001001000000000000000000000000000000000000000000000000001
```

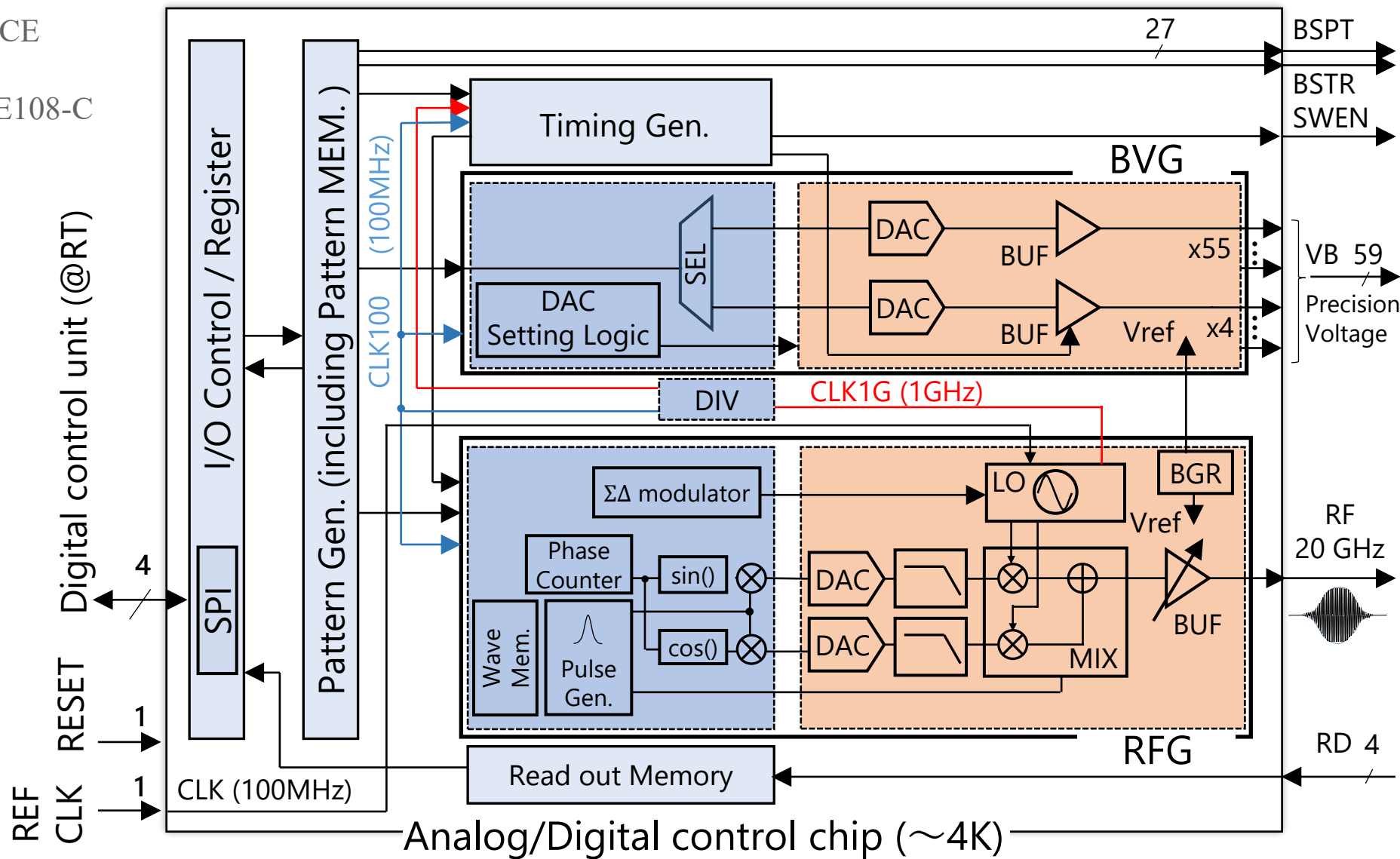
Bias pattern memory



Qubit control bias waveform

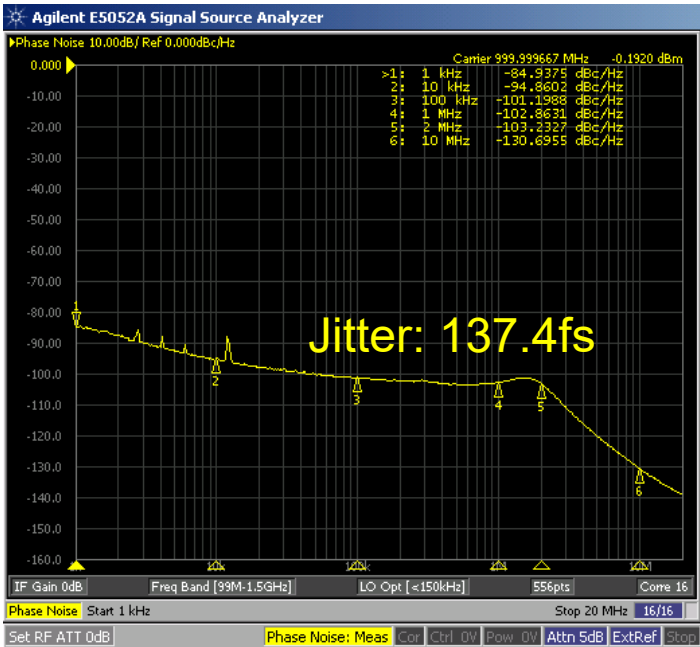
Analog/Digital control chip

T. Norimatsu *et al.*, IEICE
TRANSACTIONS on
Electronics, 2025, Vol.E108-C
No.10, pp.536-544

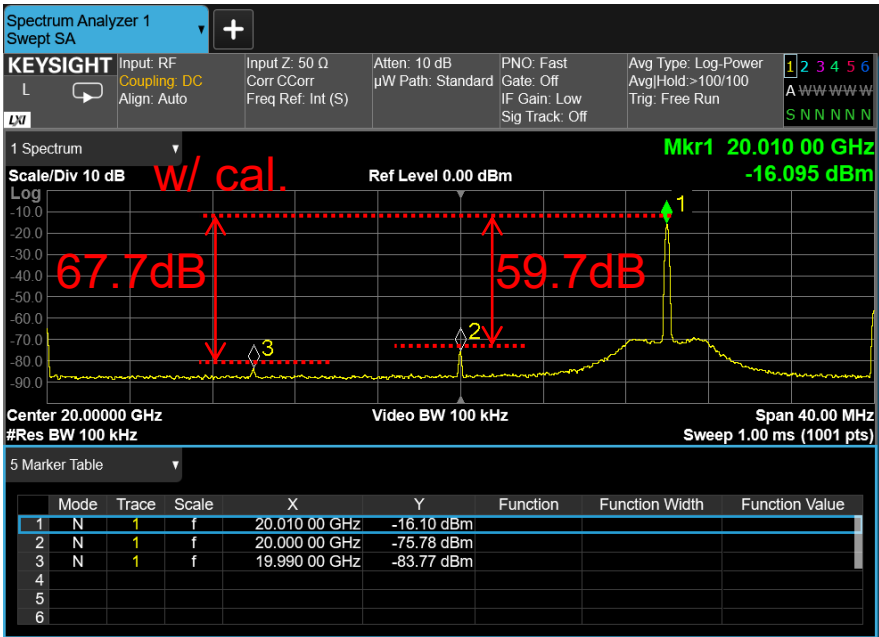


Analog/Digital control chip (RF Generator)

20 GHz LO jitter as low as 137.4fs



Calibrated LO leakage and image rejection

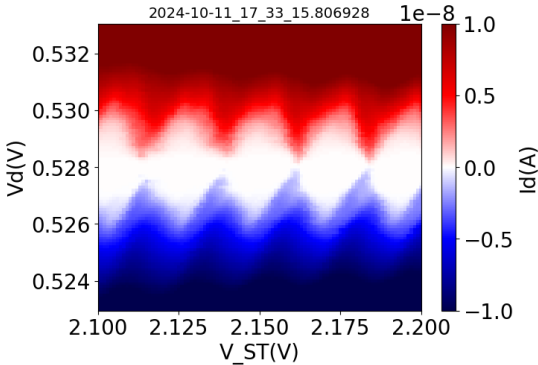
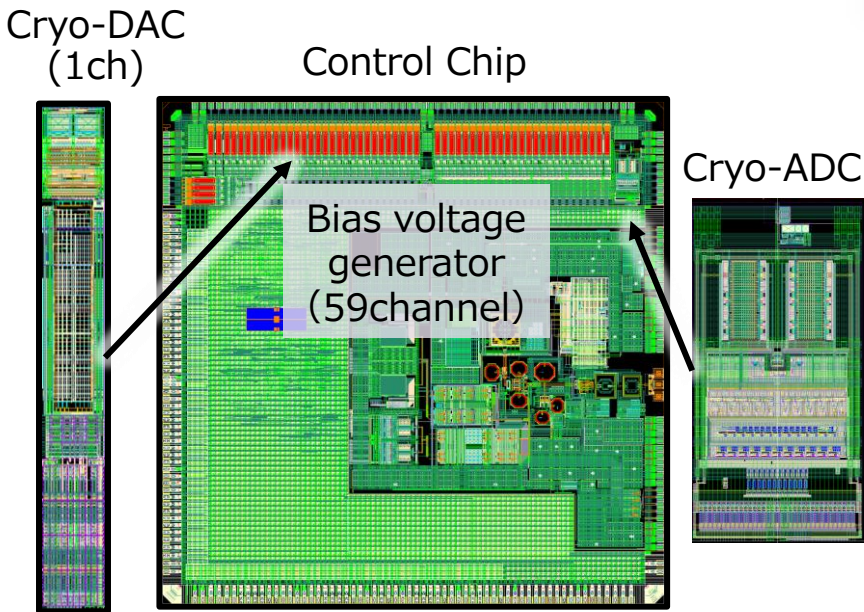
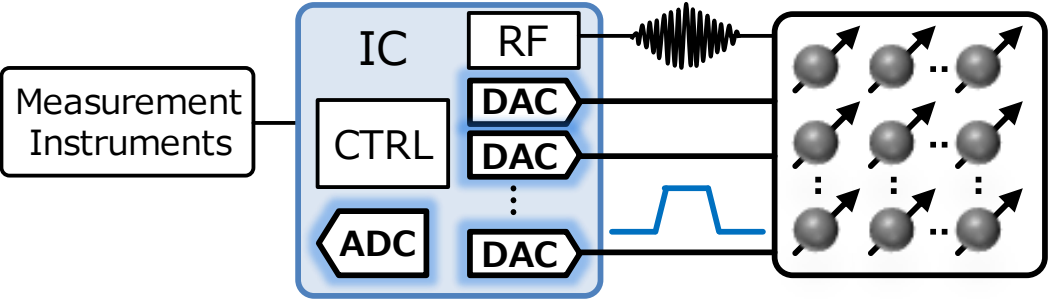


Y. Wachi, *et al.*, 50th IEEE European Solid-State Electronics Research Conference, 2024, pp.317–320

T. Norimatsu *et al.*, IEICE TRANSACTIONS on Electronics, 2025, Vol.E108-C No.10, pp.536–544

Cryogenic RF signal generation capable of 99.93% control fidelity

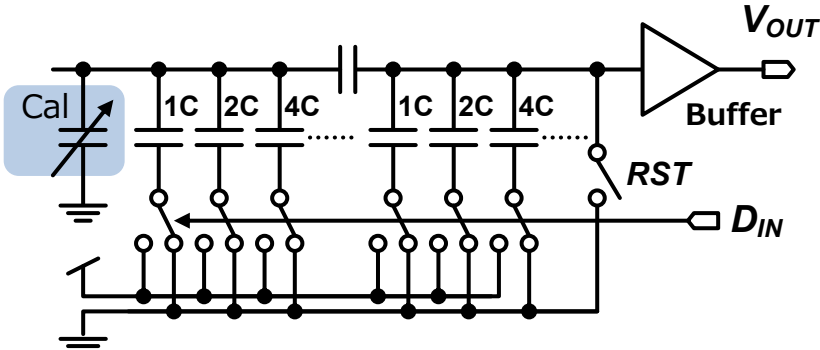
■ Development of a **cryogenic digital-to-analog converter (Cryo-DAC)**



Column diamonds

■ Cryo-DAC target specification

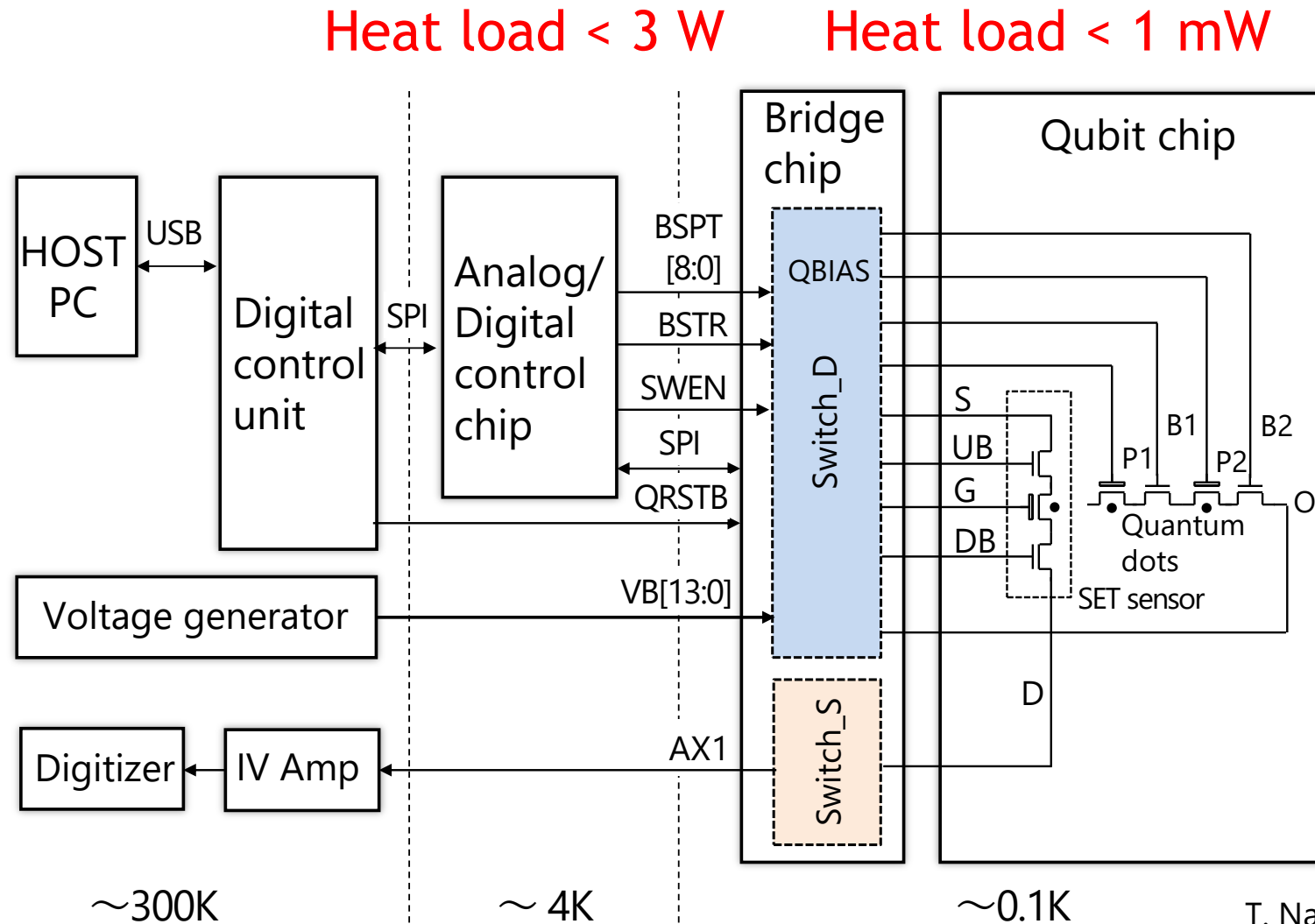
- 16bit (40uV/LSB)
- Small area (0.02 mm²/ch) for 59ch
- Low power consumption
- Calibration technique for mismatch



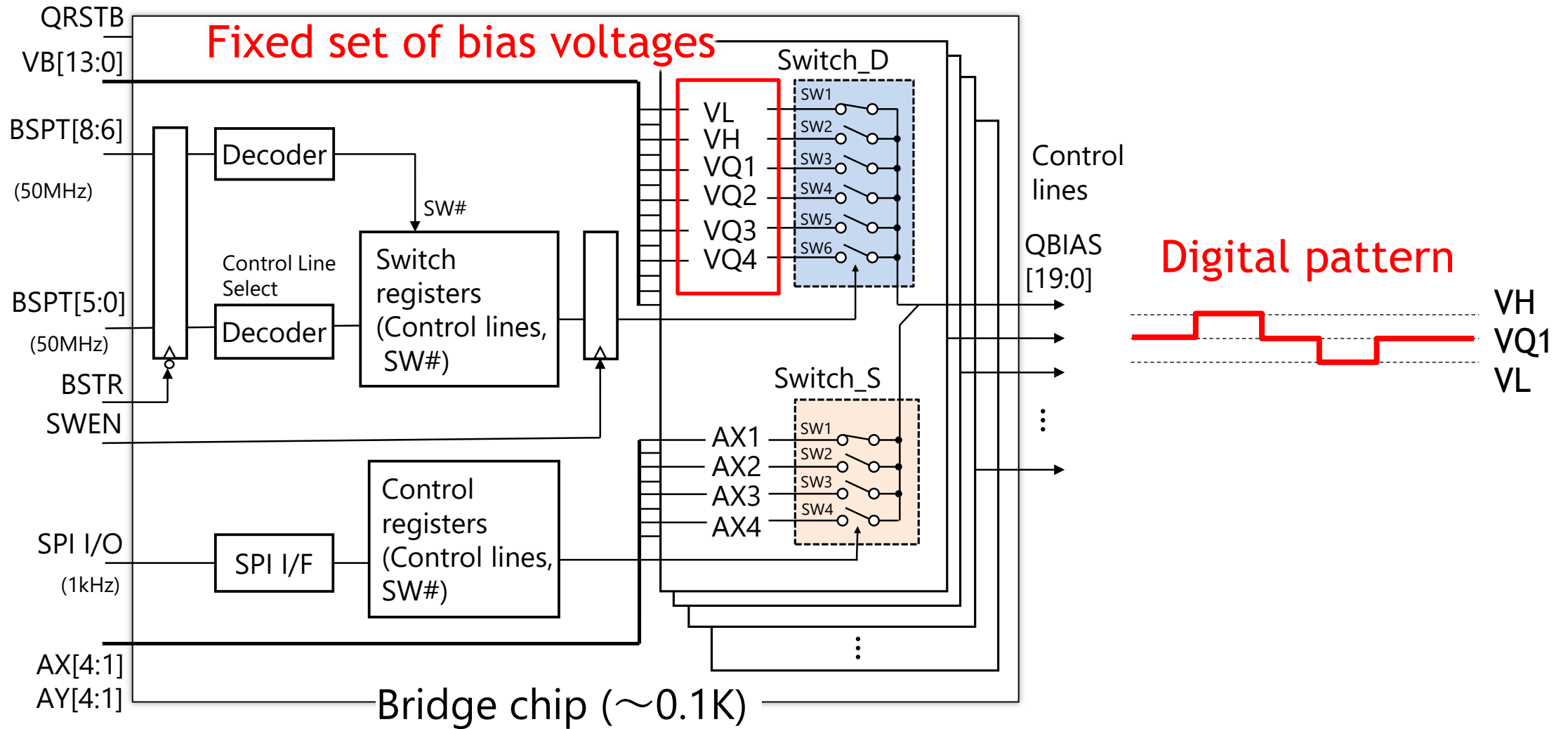
Spec. of Prototype chip *Miki, IEICE ELEX 2022*

	This work	Julich 2020	Leti 2020	UNSW 2017
Technology	40 nm CMOS	65 nm CMOS	28 nm FDSOI	0.5 μ m SOS
Architecture	Charge Redistribution	Charge Redistribution	Current Steering	Current Steering
Temperature	4 K	6 K	4.2 K	4.2 K
Supply	2.5 / 0.9 V	2.5 / 1.2 V	1.8 / 1 V	3 V
Resolution	11-bit	13-bit	8-bit	6-bit
Power	5.8 μ W	2.6 μ W	7 μ W	3.1 mW
Area	0.008 mm ²	0.0175 mm ²	0.04 mm ²	0.012 mm ²

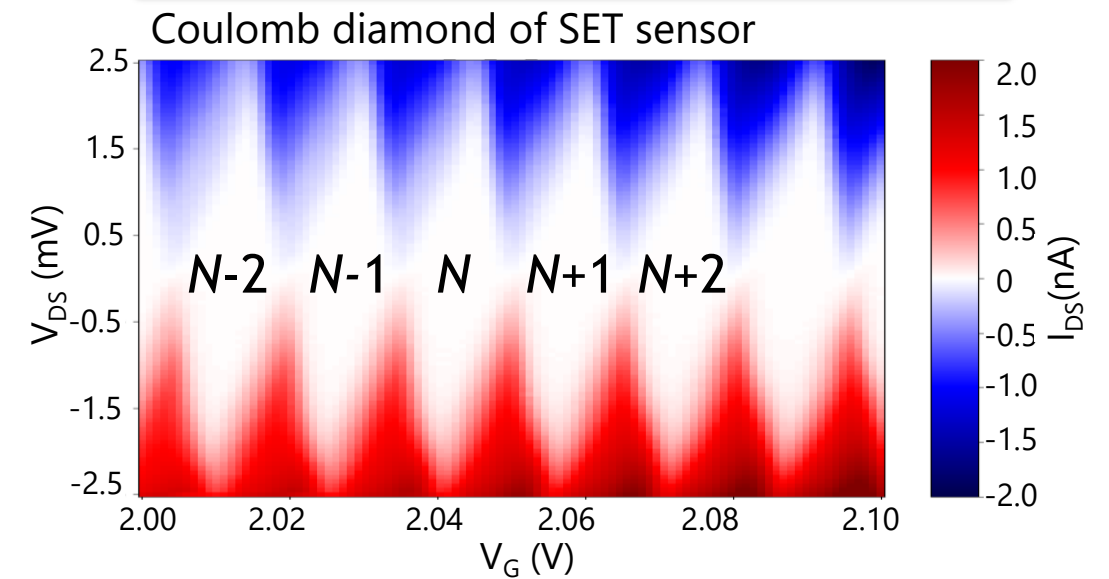
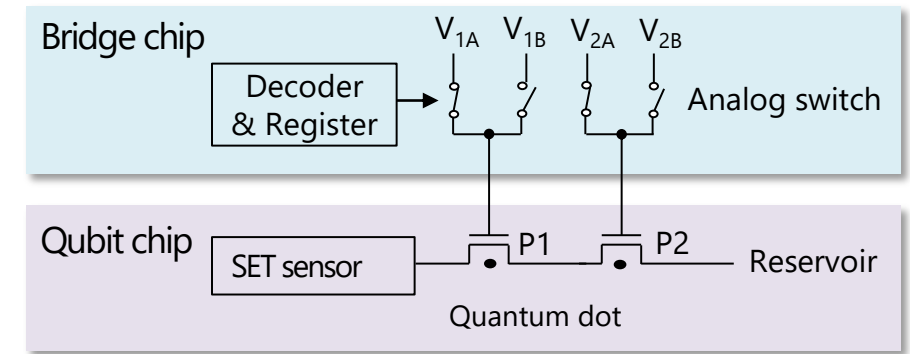
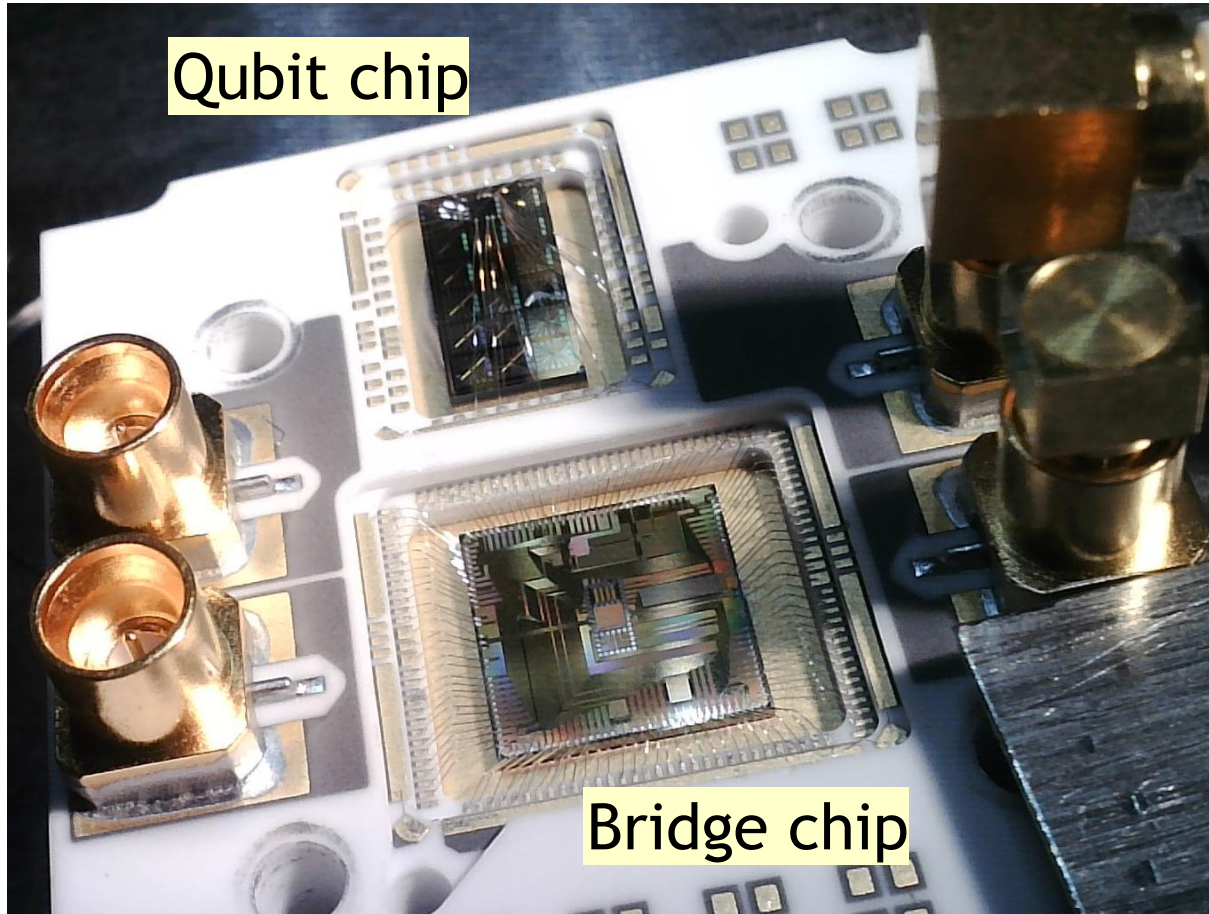
Implementation of the hierarchical architecture



Bridge chip

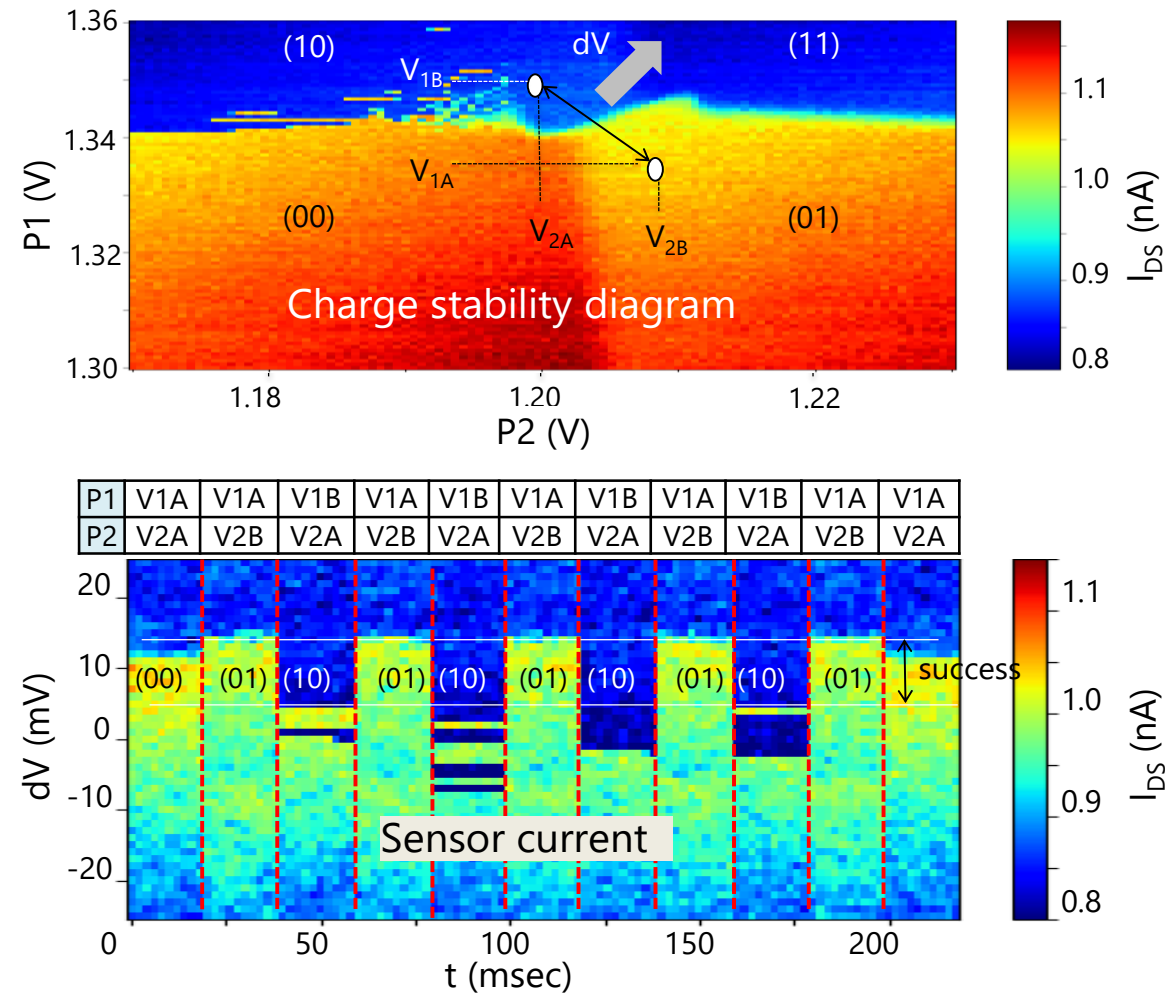


Verification of the bridge chip



Qubit chip connected to the bridge chip is controlled and measured

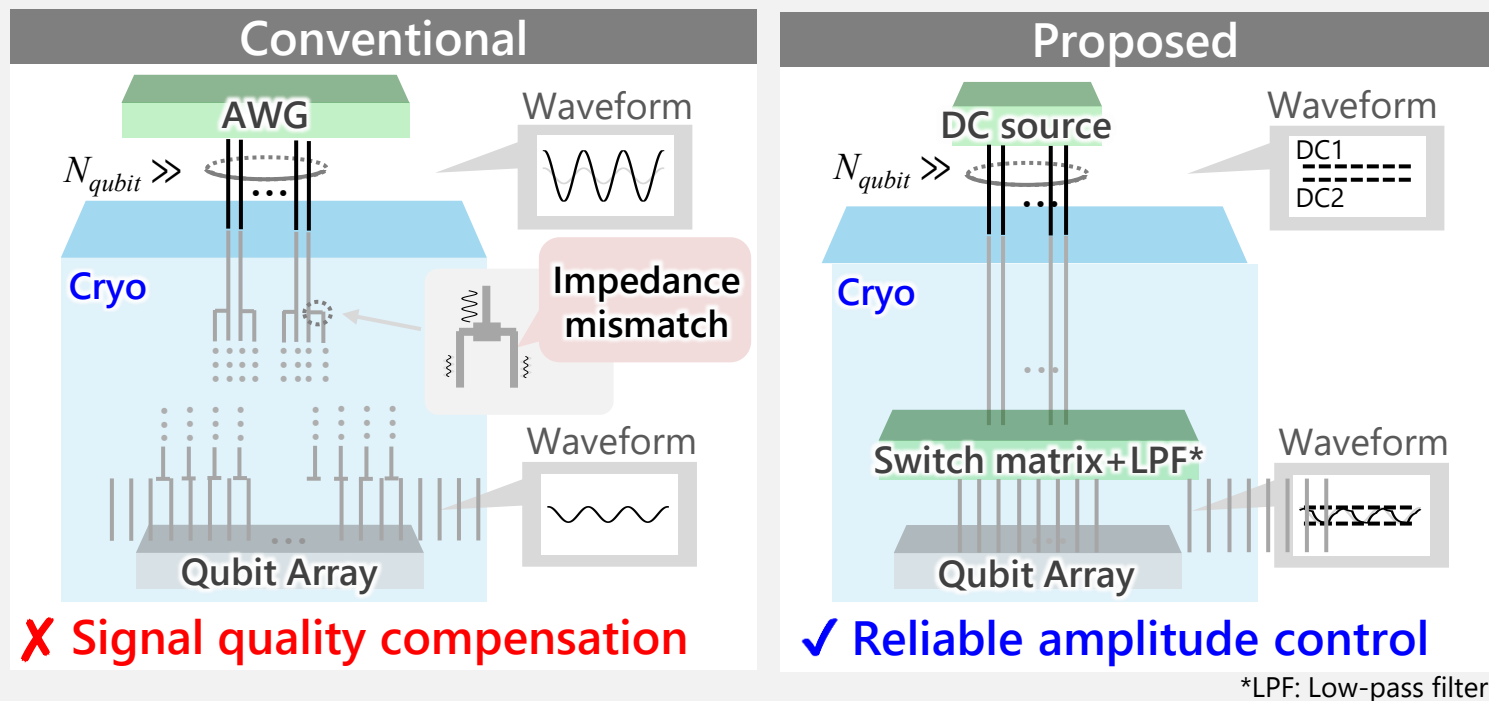
Control with the cryogenic bridge chip



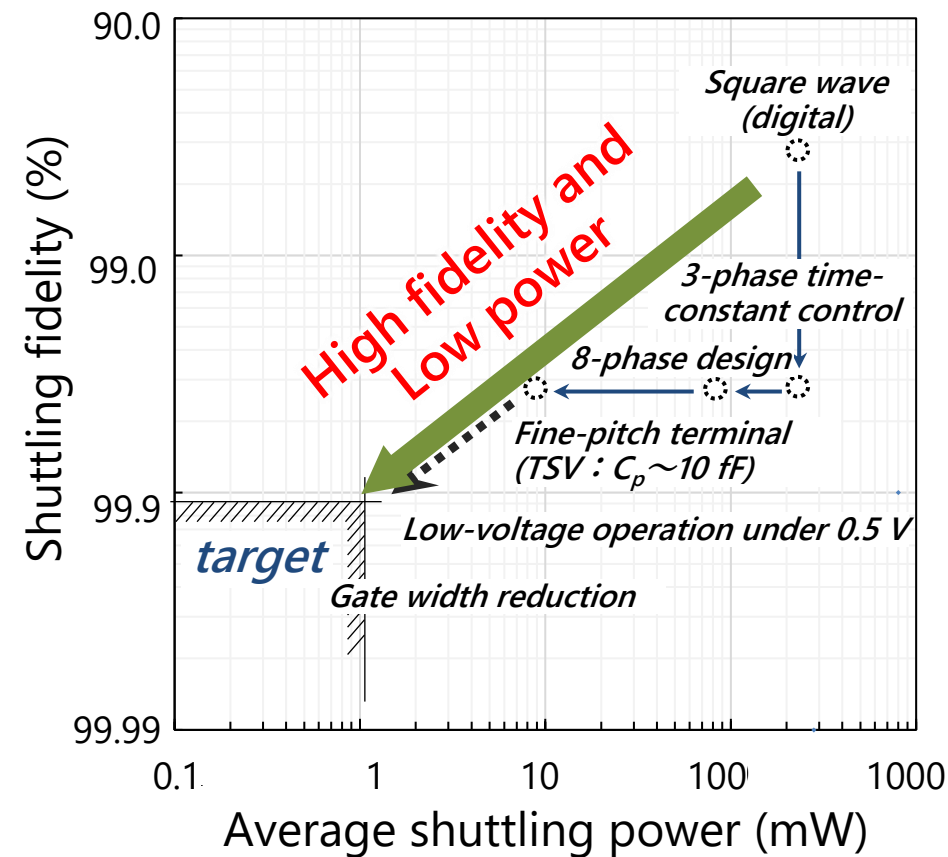
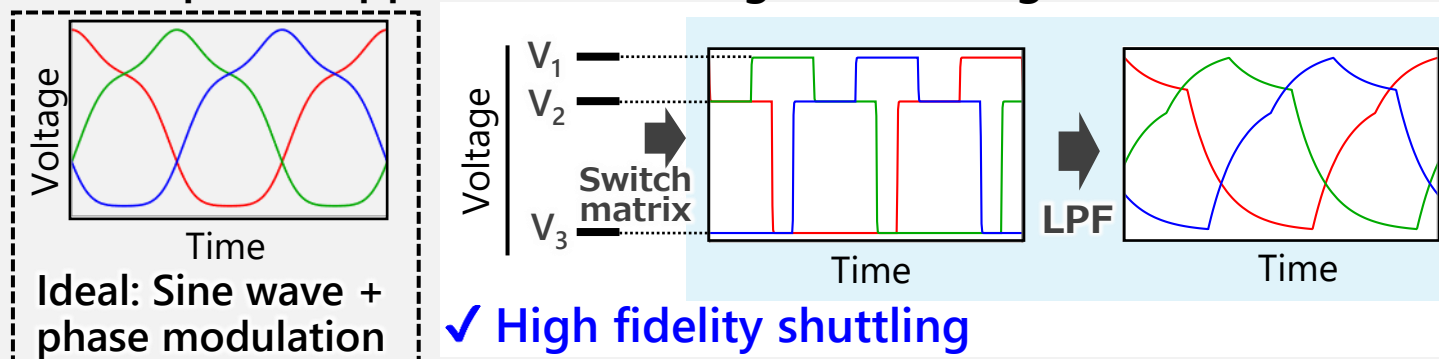
Electron occupation of the qubit chip is digitally controlled via the bridge chip

Power-efficient shuttling control system

- The generation of complicated signals required for shuttling operations is a challenge.



Low-power approximate analog waveform generation



Summary

- We are developing **computer system** based on the results of **fundamental research** of high-fidelity qubit operations in collaboration with academia.
- Cryo-CMOS chips were developed for large-scale integration of qubits that will bring breakthroughs to the system.
- A new Qubit chip configuration was proposed to implement QEC with Shuttling operation.
- Hierarchical architecture with cryo-electronics was implemented which is utilized for efficient qubit control.

Acknowledgements: Quantum computing development is supported by JST Grant No. JPMJMS2065.