



Silicon to Qubits: Soitec's FDSOI substrate powers quantum computing roadmap

23 September 2026 | Paris

Agenda

- | | |
|------------|-----------------------------------|
| 01. | The baseline: FDSOI Substrate HVM |
| 02. | 28Silicon for QuBits |
| 03. | 28FDSOI upgrade |
| 04. | Next steps |



LEVERAGING MATERIALS SCIENCES TO ENABLE UNIQUE APPLICATIONS

Leverage MATERIALS INTRINSIC PROPERTIES



Develop TECHNOLOGY SOLUTIONS



Smart Cut™



Interface engineering



Epitaxy



Advanced processing

Design ENGINEERED SUBSTRATES

- SOI product portfolio
- Anything-on-Anything (active layer on substrate)



Enable NEW PROPERTIES, ENHANCED PERFORMANCE, IMPROVED ENERGY CONSUMPTION

Connectivity

Low-power computing

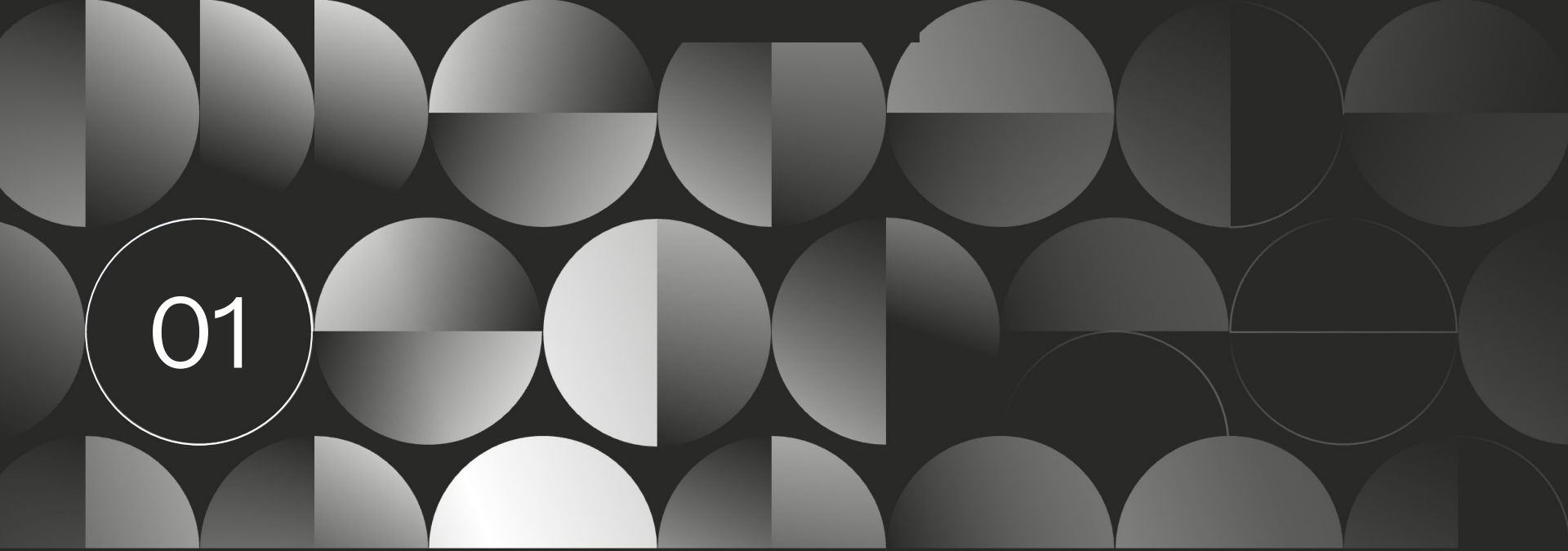
Energy efficiency

Electric vehicles

Quantum computing

3D integration

Data rate & bandwidth



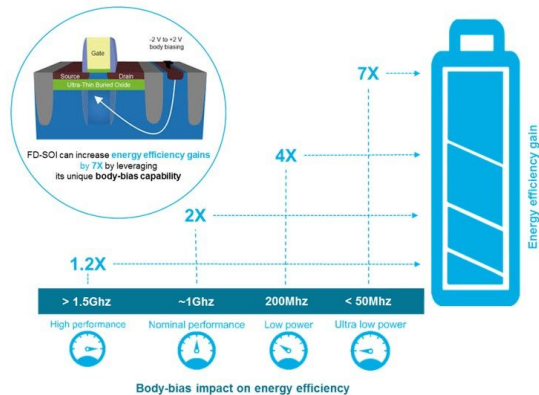
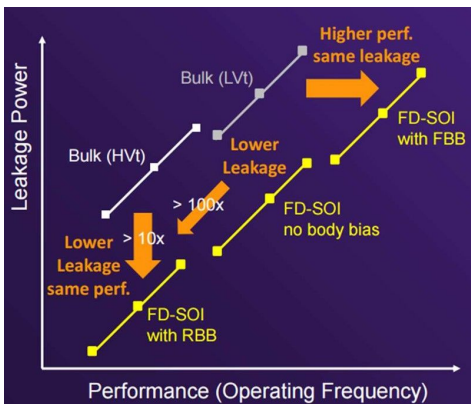
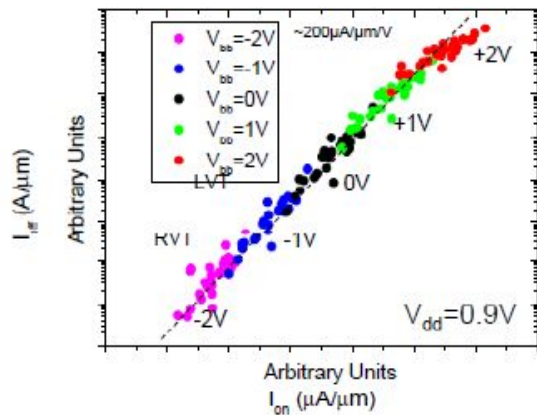
01

The baseline

FDSOI substrate HVM

UTBB FD-SOI

Benefits of FD-SOI and unique back-bias

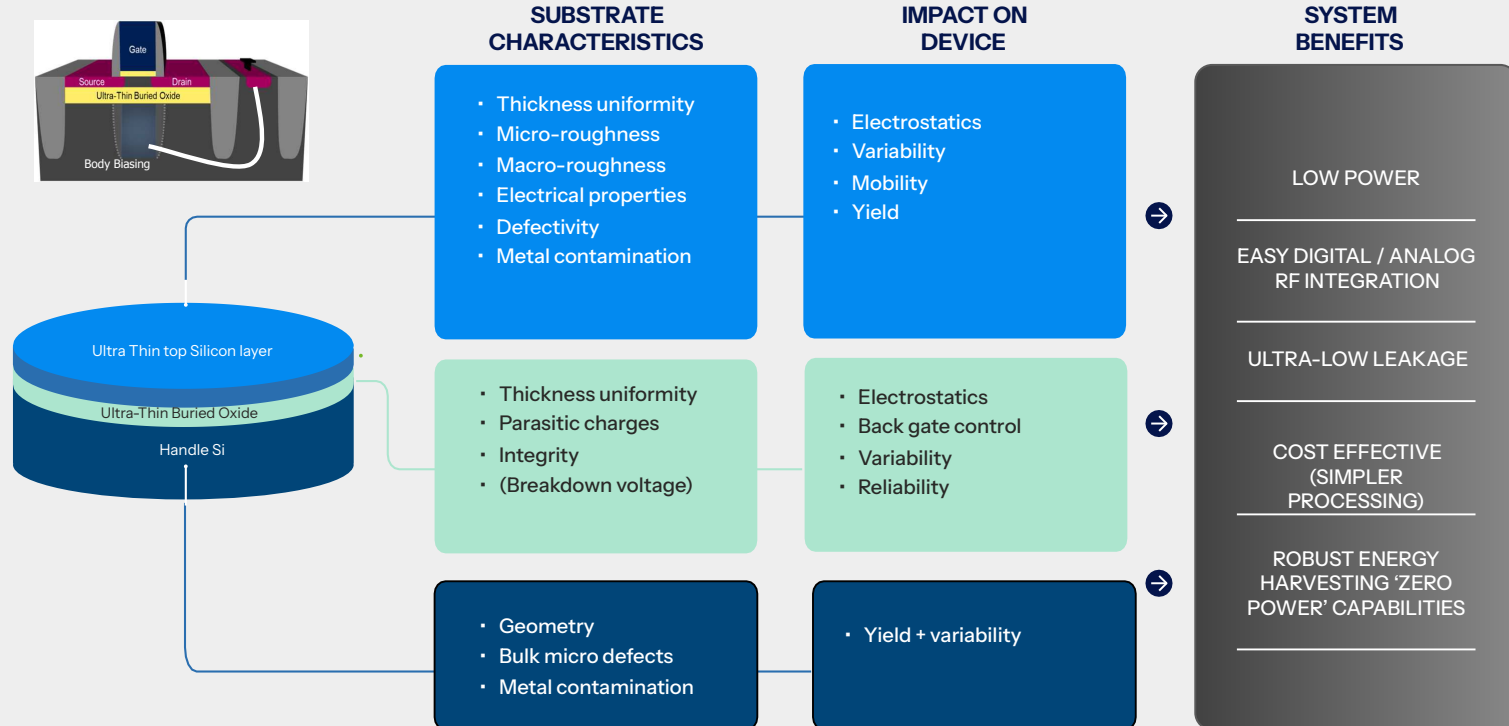


Active device layer management - FDSOI

Performance already embedded in the substrate

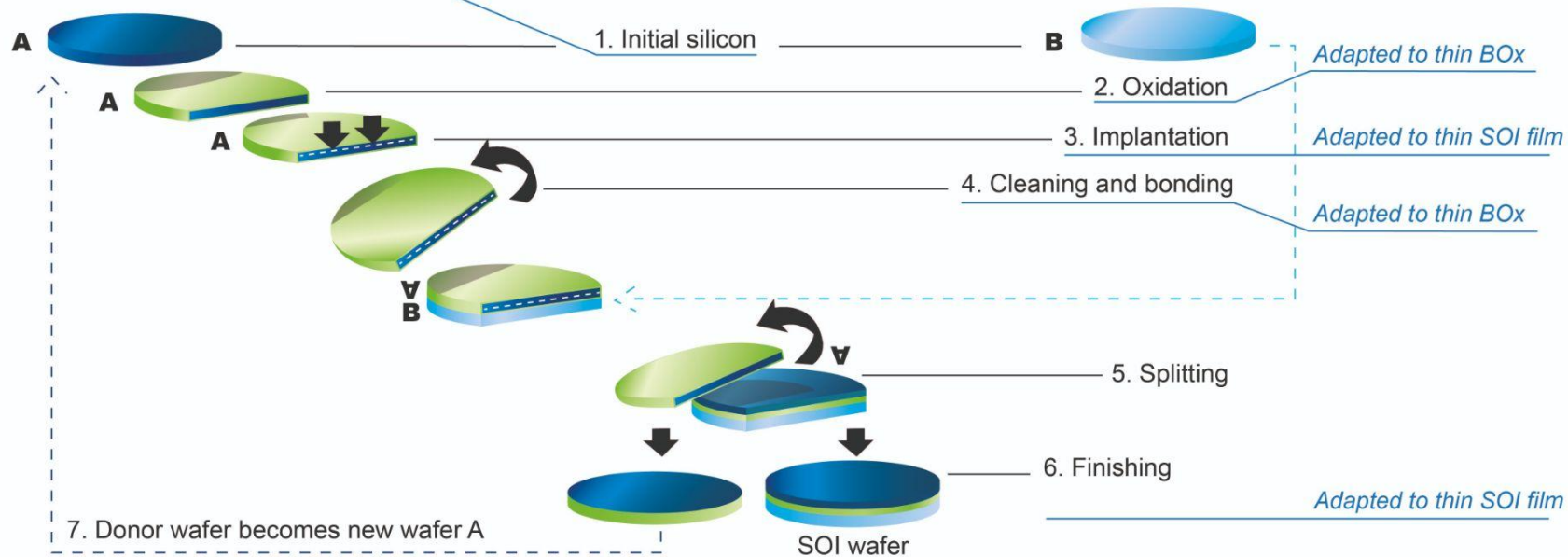
Knobs to control Perf/Power:

- Gate bias
- Back Bias



Smartcut™ process tailored for FDSOI

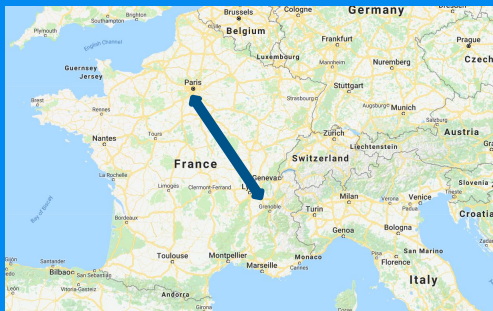
*High-quality top wafer for
thin SOI film compatibility*



FDSOI enabler

Thickness control at atomic level in HVM

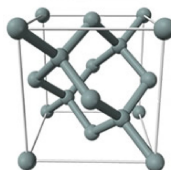
Grenoble- Paris
~ 480 km



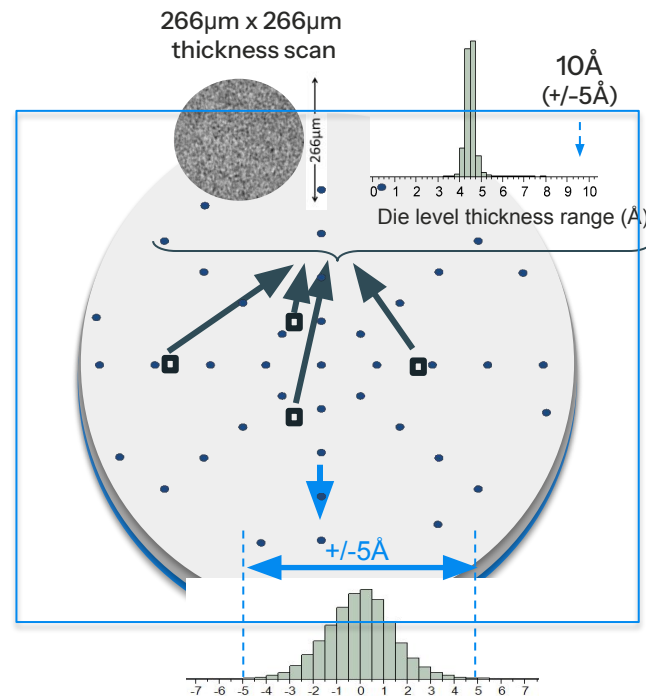
$\pm 0.8\text{mm}$ 

Millions wafers
controlled at
atomic level, all
points, all wafers

$\pm 5 \text{ \AA}$

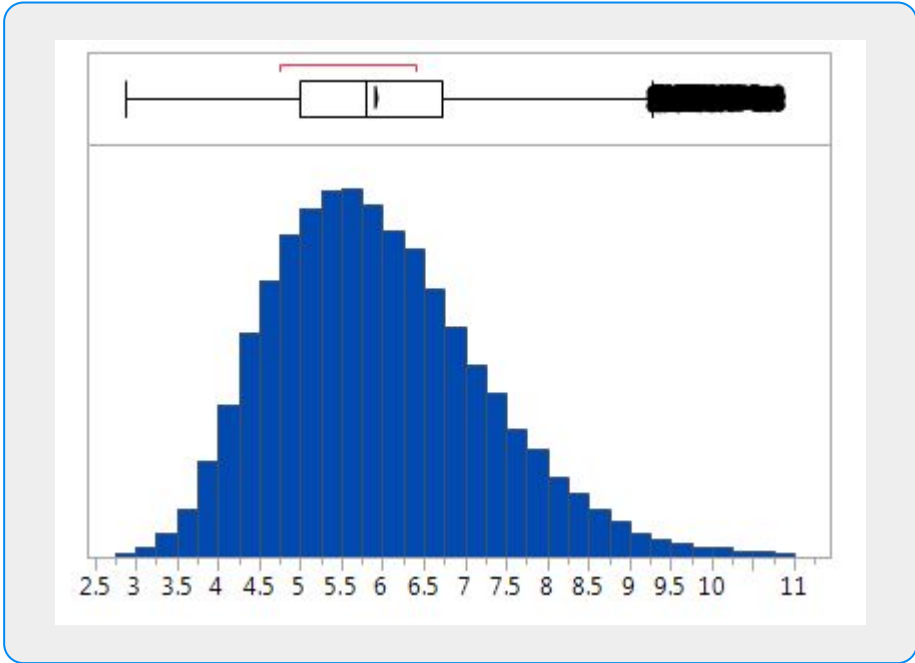


Mature process
and yield in HVM



Atomic level control in HVM mode

FD GEN1 - Tsi range distribution



Quantiles

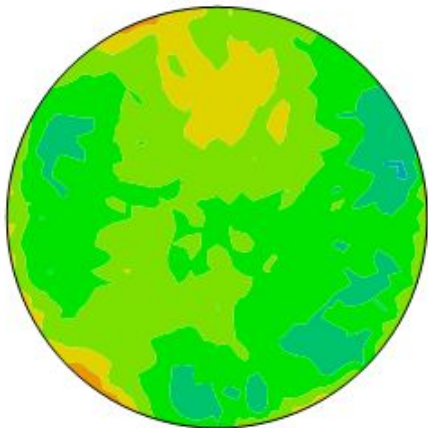
100.0%	maximum	10.833
99.5%		9.7
97.5%		8.647199
90.0%		7.5764
75.0%	quartile	6.678
50.0%	median	5.76
25.0%	quartile	4.97
10.0%		4.39
2.5%		3.8409
0.5%		3.3941882
0.0%	minimum	2.875

Summary statistics

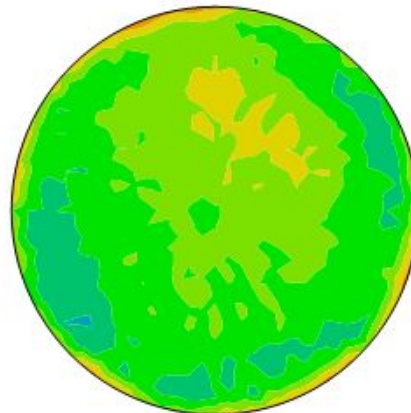
Mean	5.8924187
Std Dev	1.2479579
Std Err Mean	0.0052814
Upper 95% Mean	5.9027703
Lower 95% Mean	5.8820672
N	55835

Atomic level control in HVM mode

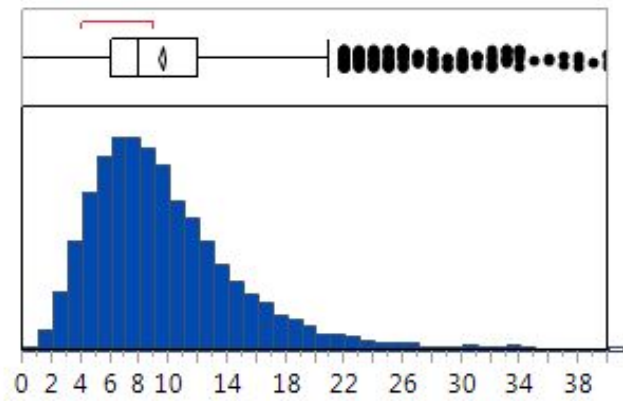
Statistical Analysis
Std Dev= 0.87A



Range Analysis
Range Tsi = 5.07A



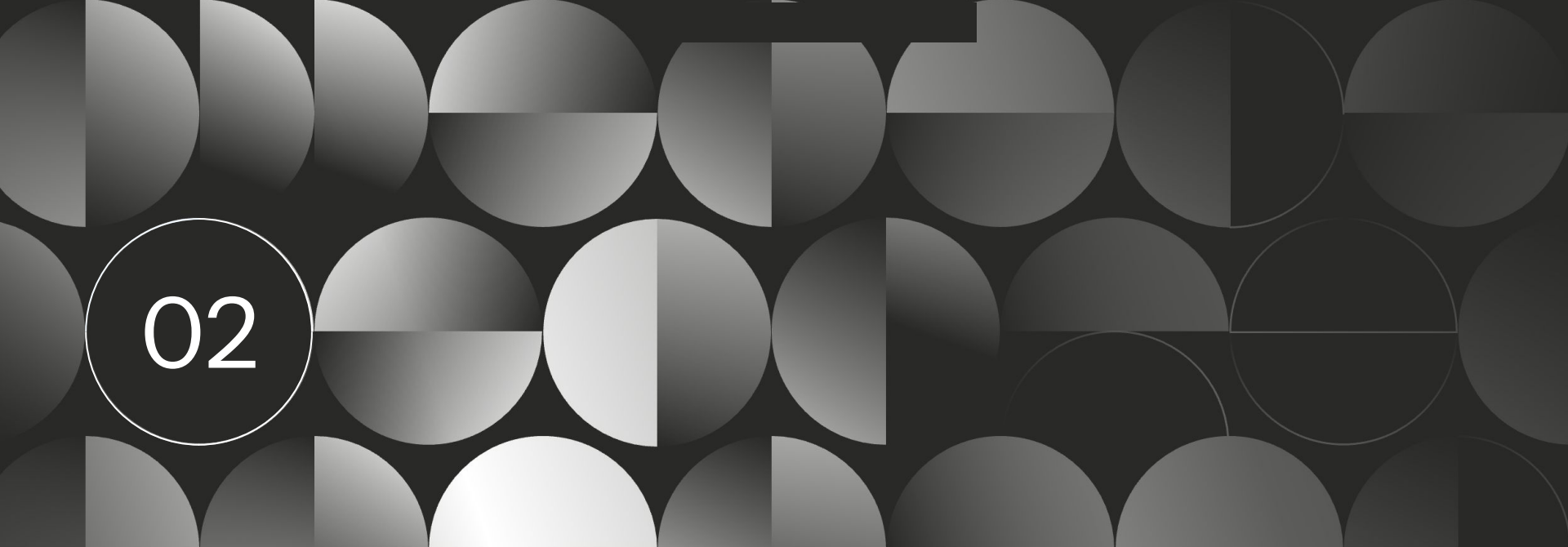
12nm top silicon layer integrity monitored at 32nm threshold



Quantiles		
100.0%	maximum	265
99.5%		45
97.5%		24
90.0%		16
75.0%	quartile	12
50.0%	median	8
25.0%	quartile	6
10.0%		4
2.5%		2
0.5%		1
0.0%	minimum	0

Summary statistics	
Mean	9.4587033
Std Dev	7.6297673
Std Err Mean	0.0884912
Upper 95% Mean	9.632171
Lower 95% Mean	5.8820672
N	7434





02

28Silicon for qubits

Silicon isotopes: Why ^{28}Si is essential for spin qubits

ATOMIC PHYSICS & QUANTUM NOISE

^{28}Si ENRICHED TARGET 92.2% $\rightarrow$ >99.99%



Nuclear Spin (I): $I = 0$ (Zero Spin)
Magnetic Moment: $0 \mu\text{N}$ (Inert)

Acts as a zero-noise "semiconductor vacuum". Electron spin qubits remain undisturbed.

NUCLEAR SPIN ELIMINATION

^{29}Si NOISE SOURCE 4.7% natural



Nuclear Spin (I): $I = 1/2$ (Magnetic)
Magnetic Moment: $-0.555 \mu\text{N}$

Generates random Overhauser magnetic field fluctuations, causing rapid qubit dephasing.

OVERHAUSER DEPHASING SOURCE

^{30}Si INERT TRACE 3.1% natural



Nuclear Spin (I): $I = 0$ (Zero Spin)
Magnetic Moment: $0 \mu\text{N}$ (Inert)

Magnetically quiet, but filtered alongside ^{29}Si during mass centrifugation.

NATURAL SILICON (4.7% ^{29}Si)

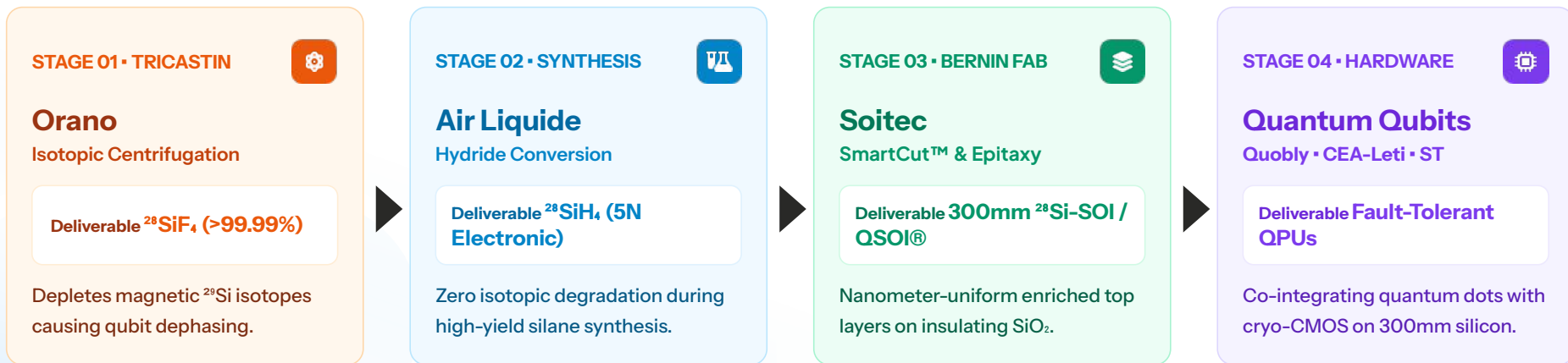
Coherence $T_2^* \approx 1 \mu\text{s}$ • Gate Fidelity < 98%

10,000× GAIN

PURIFIED ^{28}Si (>99.99% / <50 PPM ^{29}Si)

Coherence $T_2^* > 10 \text{ ms}$ • Gate Fidelity > 99.9%

^{28}Si Journey: From Nuclear Centrifuge to Quantum Qubits



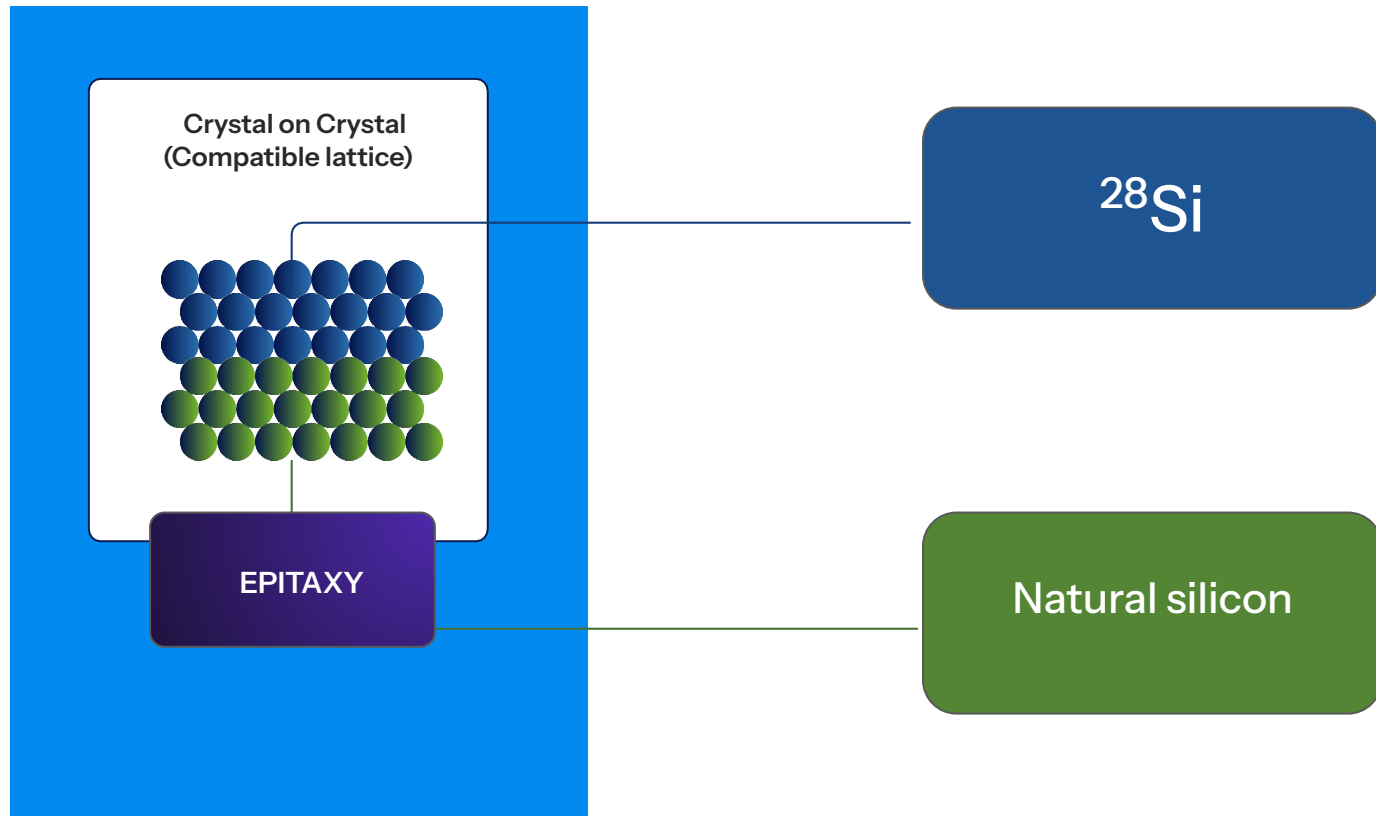
SOVEREIGN DEEP-TECH VALUE CHAIN

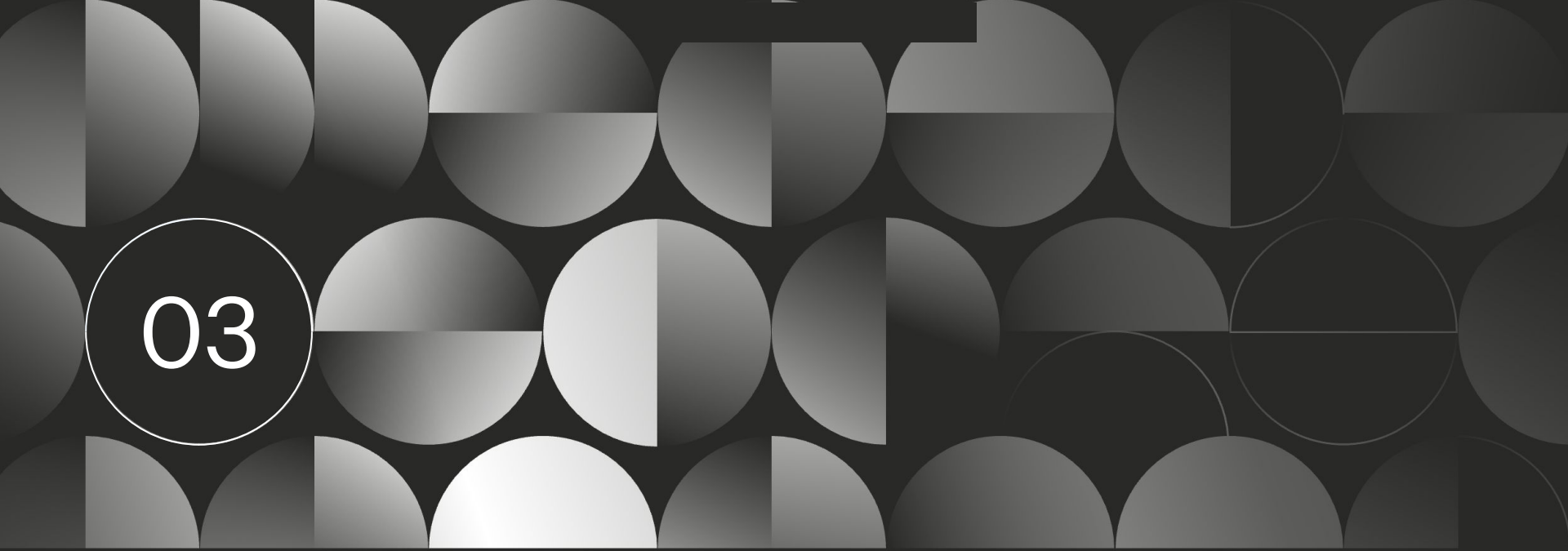
100% EUROPEAN SOURCING

STRATEGIC AUTONOMY ARCHITECTURE

- Zero Nuclear Spin Noise (>99.99% Isotopic Purity)
- Standard 300mm CMOS Foundry Processing
- Scale to Million-Qubit Architectures

Preparing materials for donor and base wafers



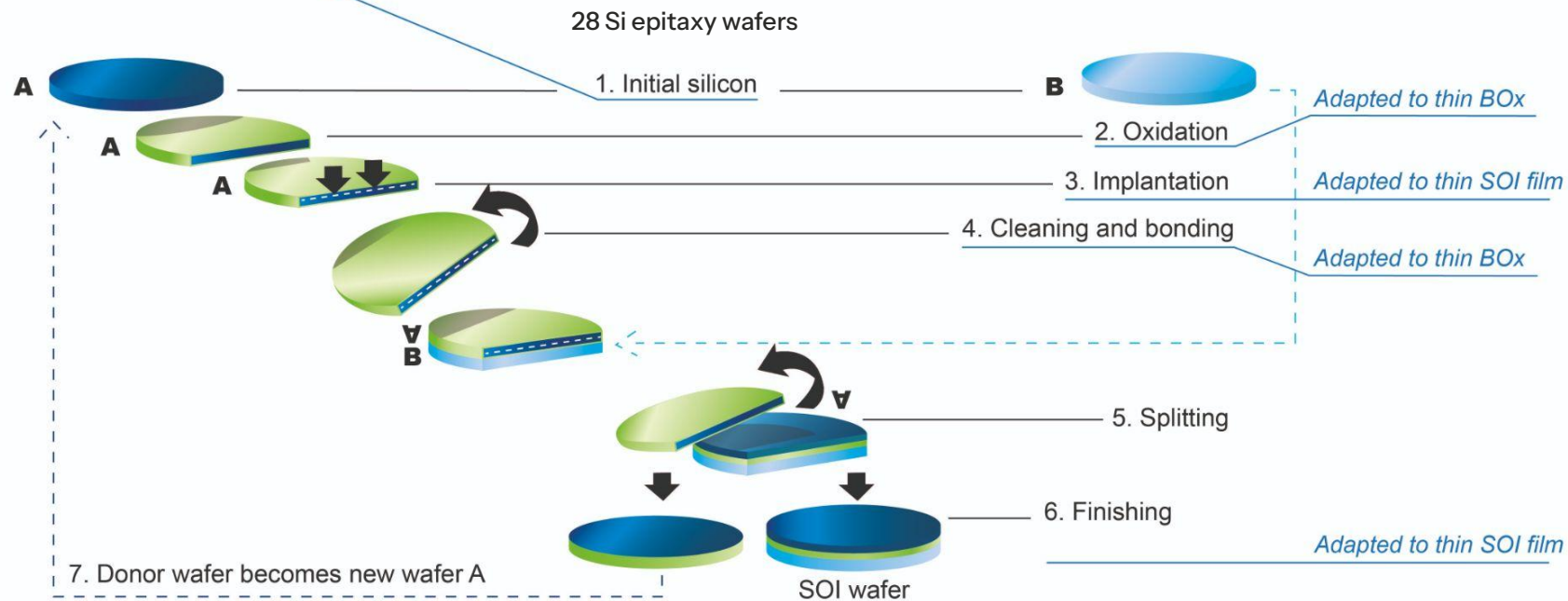


03

28FDSOI upgrade

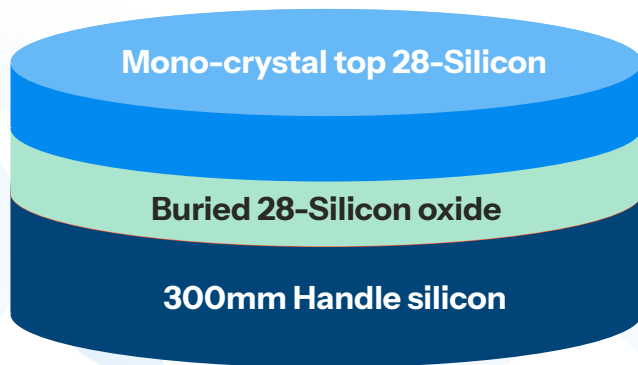
28Si Upgrade of FDSOI SmartCut™

*High-quality top wafer for
thin SOI film compatibility*



FD-²⁸SOI Product

The perfect platform for spin qubits already exists

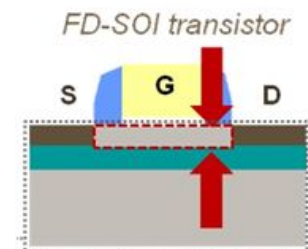


“

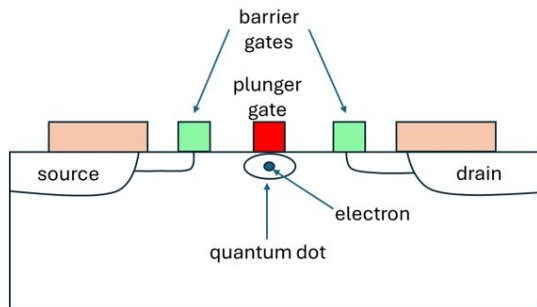
Fully Depleted - ²⁸SOI

No mobile free carrier, no nuclear spin, high processability

Benefits of FDSOI electrostatics control and no nuclear spin

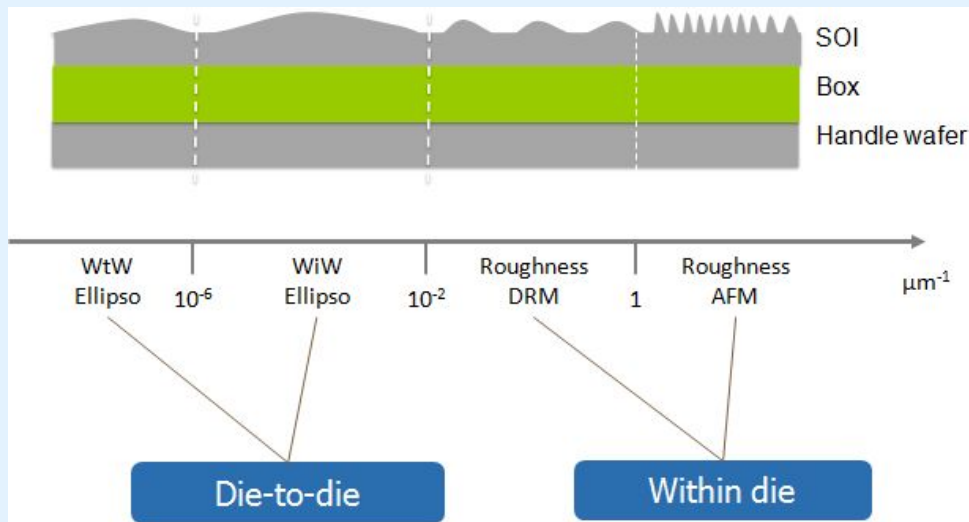


Channel thickness is critical



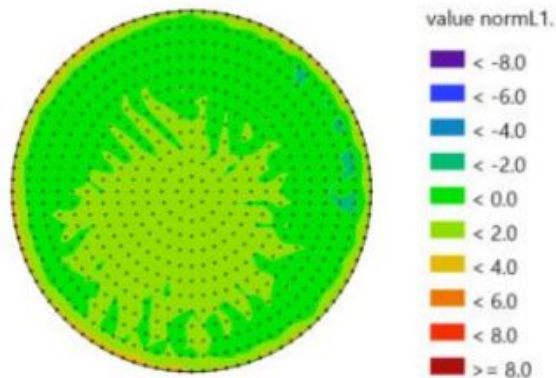
Silicon qubit transistor (simplified)

All spatial frequencies considered in order for IC makers to get same device performances

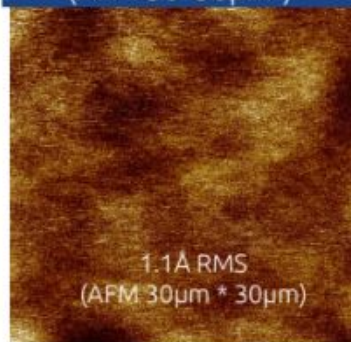


High uniformity for Qubits

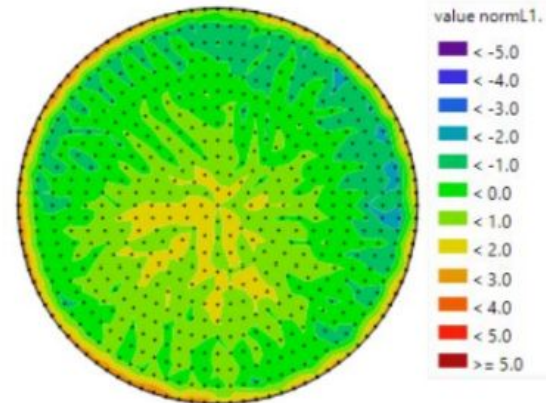
Thickness Wafer map (Å)



SOI roughness
(AFM 30*30 μm^2)

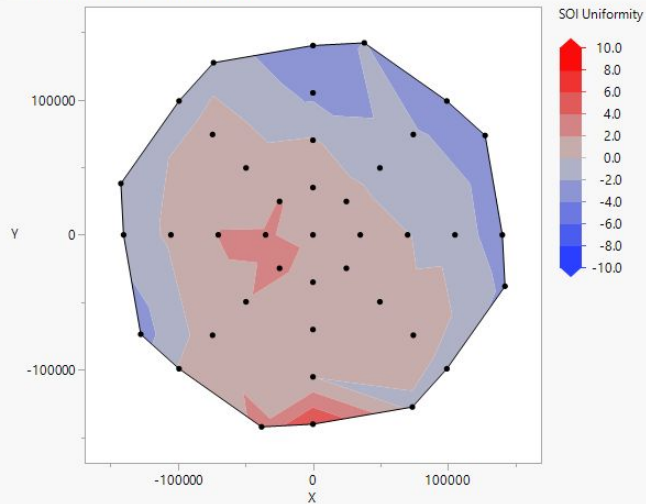


BOX Thickness map (Å)

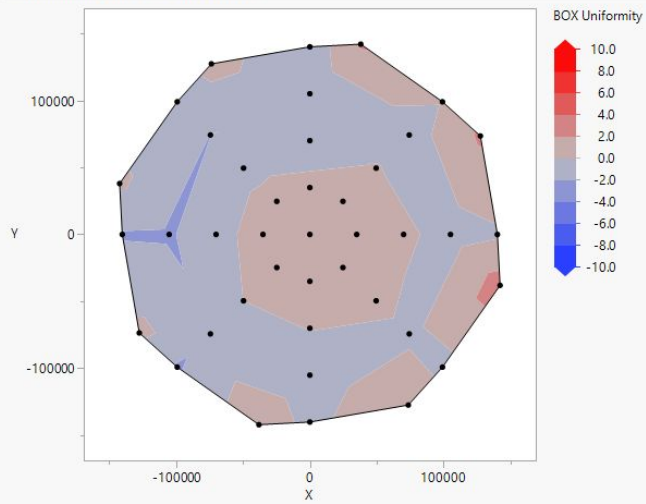


FD-²⁸SOI uniformity

Contour Plot for SOI Uniformity

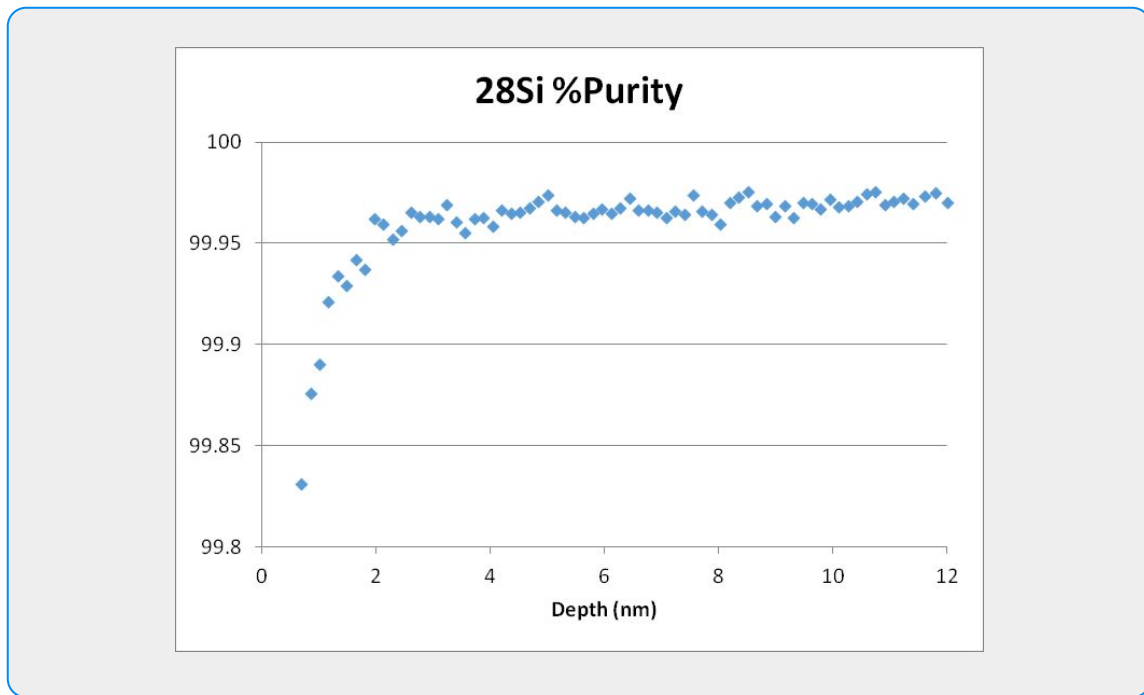


Contour Plot for BOX Uniformity

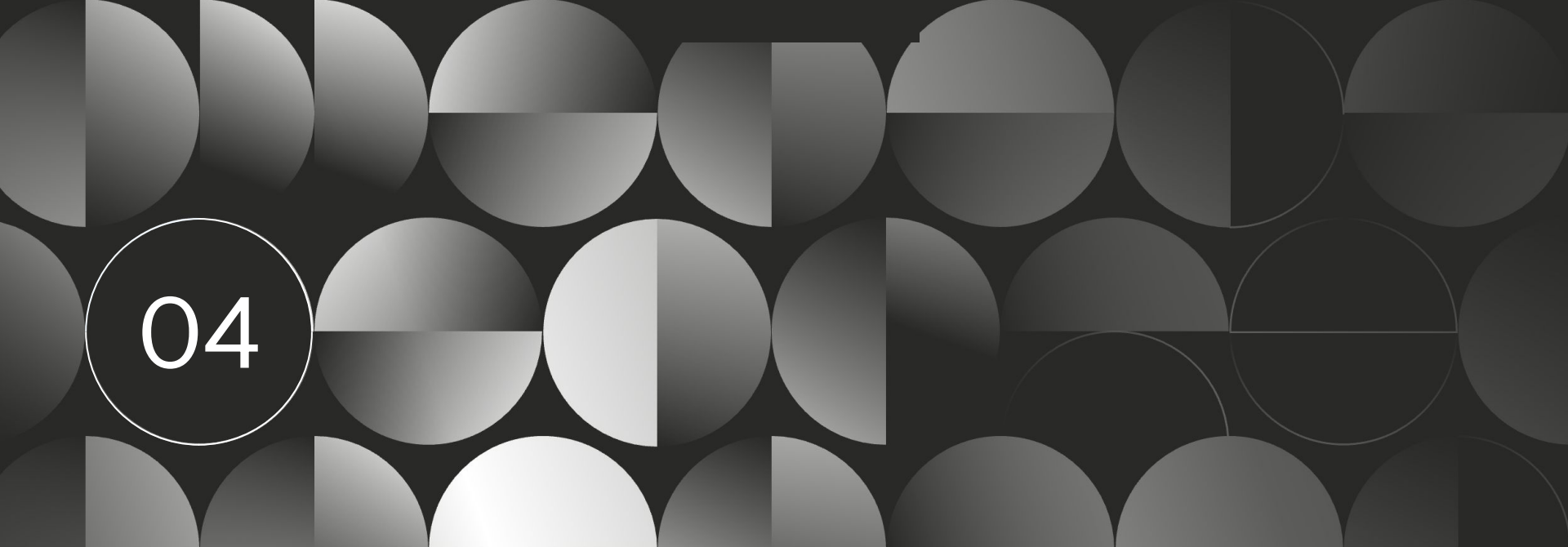


R&D samples already yields lattice level uniformity across the 300mm wafers

FD-²⁸SOI Purity



High isotopic purity maintained during our SOI process



04

Next steps

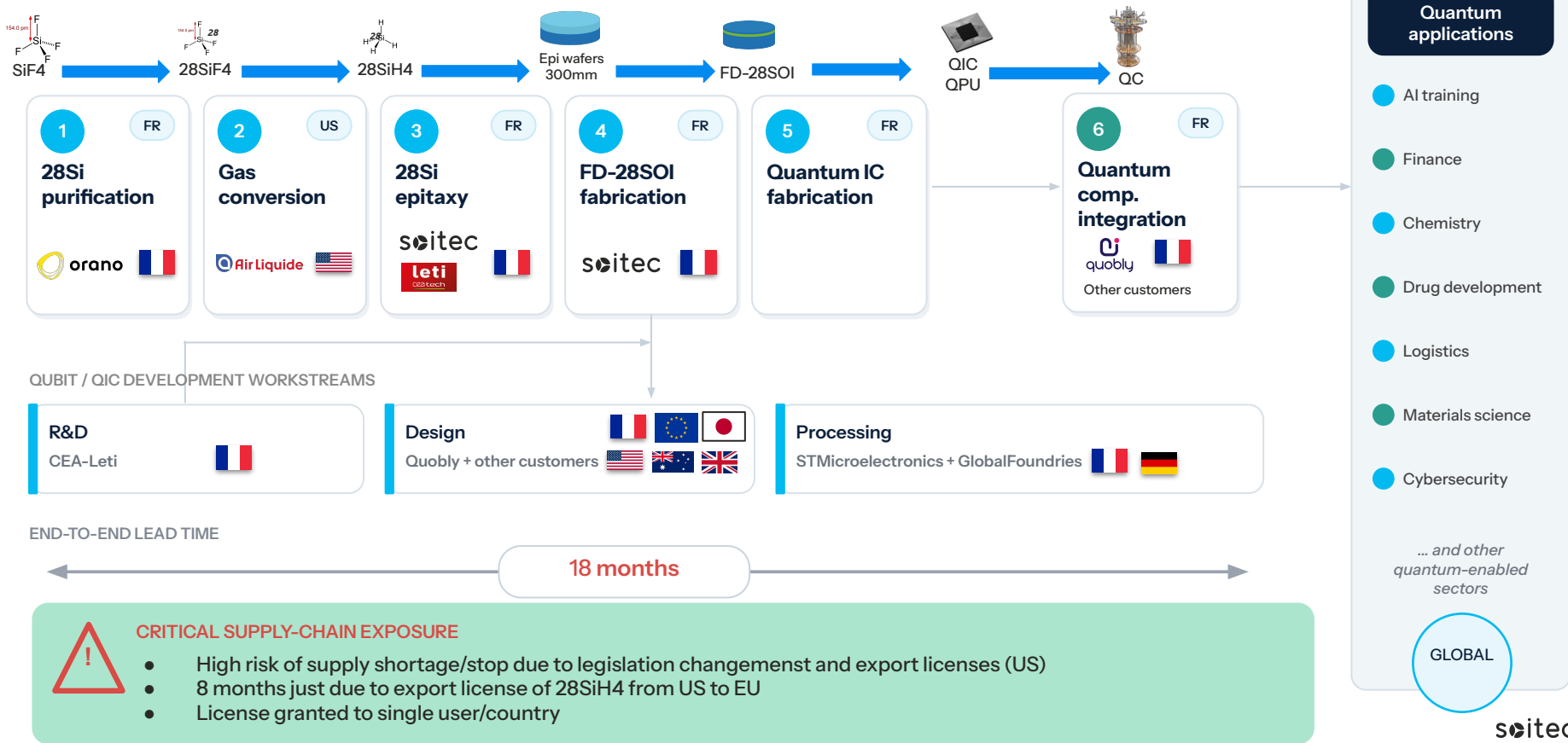
FD-SOI scaling: 28nm to single-digit nodes

Node Tier	STMicroelectronics	GlobalFoundries	Samsung Foundry	Key Milestones
28nm Mature Production	28nm FD-SOI (Crolles) High-volume automotive & rad-hard ePCM	<i>Skipped</i> Transitioned directly to 22nm planar platform	28FDS (Giheung S1) First commercial eMRAM and RF integration	Planar UTBB launch & dynamic body biasing
22nm Commercial Mainstream	<i>Sourced / Partnered</i> Co-developed IP with GF Dresden ecosystem	22FDX / 22FDX+ (Fab 1) \$2B+ design wins, 0.4V Vdd, 77GHz radar	<i>Skipped</i> Extended 28FDS variants straight to 18FDS	0.4V Vdd floor & FinFET-class power efficiency
18nm Next-Gen Industrial	18nm FD-SOI (Crolles) Joint mega-fab with GF; auto MCUs & eNVM	18FDX Alliance (Crolles) European 300mm capacity expansion	18FDS (Giheung) +20% speed, -40% power vs 28FDS; eMRAM + RF	Joint fab scaling & automotive qualification
12nm / 10nm Pilot / Demonstrated	10nm FD-SOI (FAMES) CEA-Leti pilot line under EU Chips Act	12FDX (Developed) Demonstrated in R&D; deprioritized for 22FDX	10nm FDS Exploration R&D vehicle modeled with CEA-Leti	4x density over 28nm, 68nm CPP, 48nm metal pitch
Single-Digit Advanced R&D		Ecosystem Research Sub-10nm evaluation with Soitec substrates		



Sources & Reference Notes: STMicroelectronics Capital Markets Day & Crolles announcements; GlobalFoundries Technology Summit (GTS 22FDX / 12FDX); Samsung Foundry Forum (SFF 28FDS / 18FDS); CEA-Leti FAMES Pilot Line (EU Chips Act); Soitec UTBB Substrate Architecture Briefs.

Towards a comprehensive ^{28}Si FDSOI supply chain driven by the EU





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