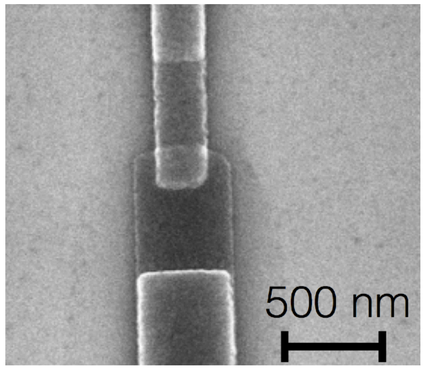
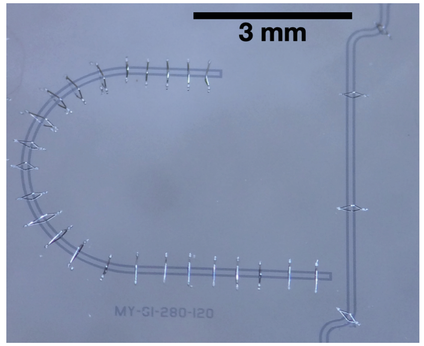
Superconducting quantum processors
What are the challenges ahead?

Benjamin Huard
Ecole Normale Supérieure de Lyon, France

Scientific advisor to Alice & Bob

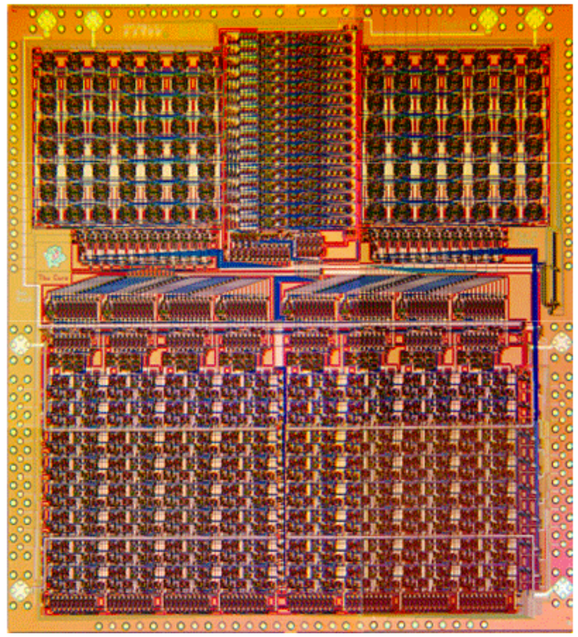




[KIDE fridges by Bluefors]

Superconducting computers

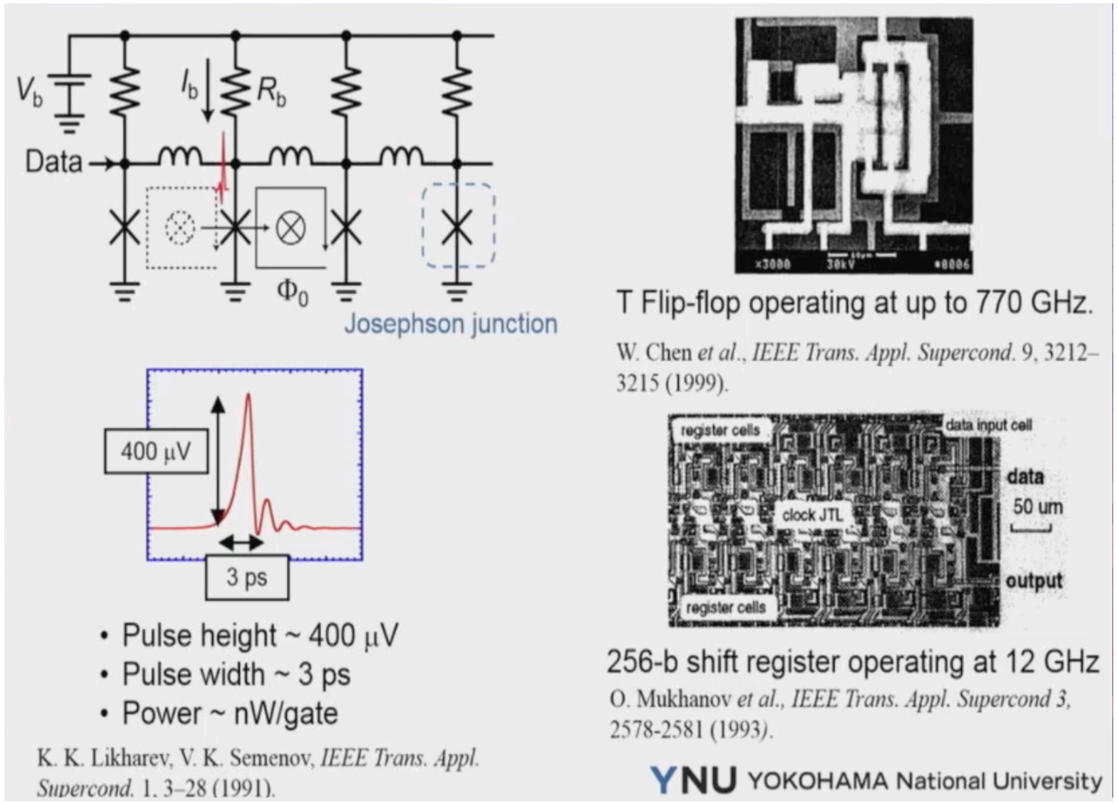
computer



FLUX-1R1: 65759 Josephson junctions

[NGST/SUNY-Stony Brook/JPL (2002)]

Rapid single flux quantum (RSFQ) circuit

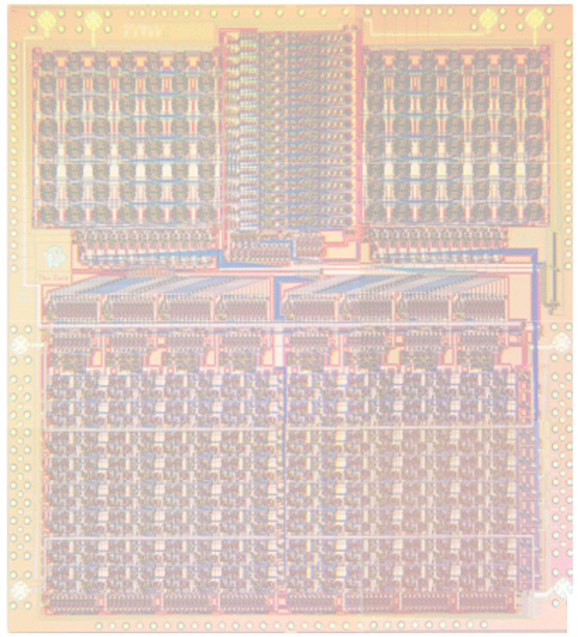


main challenges are reliable memory and scaling up

courtesy of Nobuyuki Yoshikawa

Superconducting computers

computer



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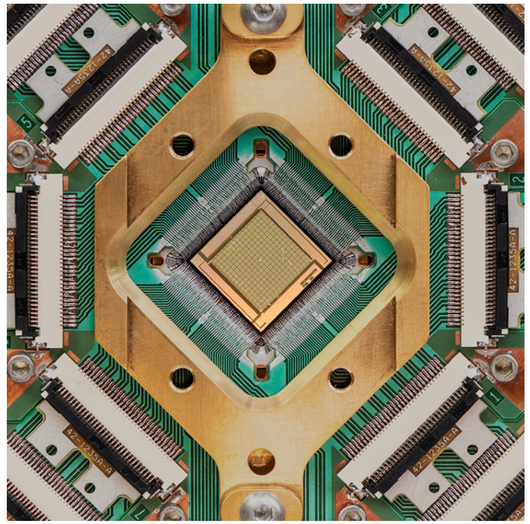
quantum annealer

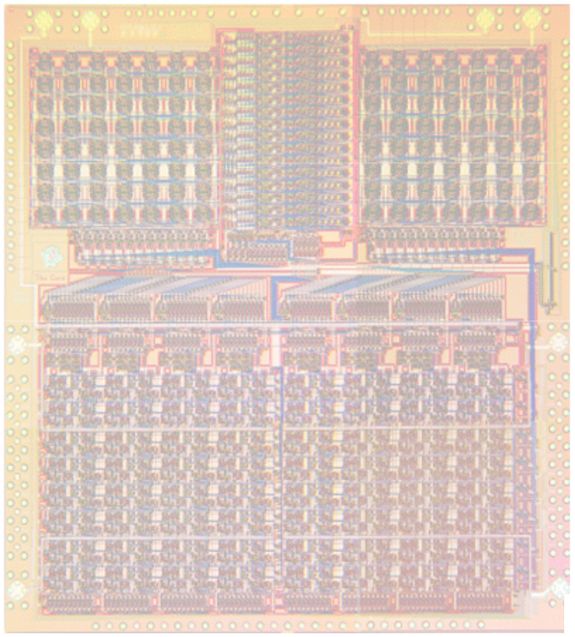


D-Wave Advantage: 5000 qubits (2021)

«quantum computer»

Superconducting computers

classical computer



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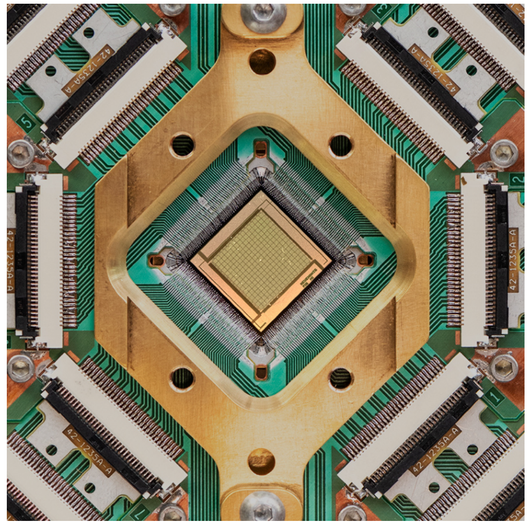
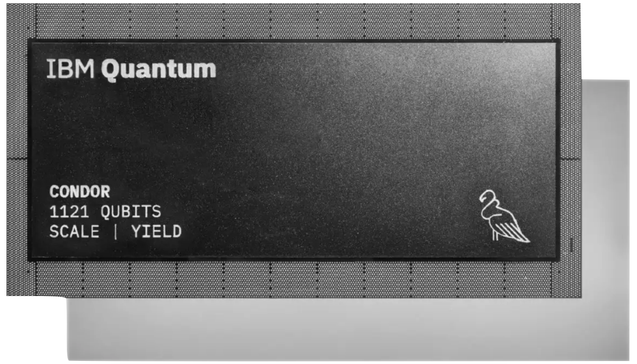


D-Wave Advantage: 5000 qubits
(2021)

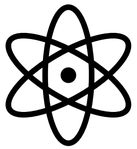
gate based
quantum processor



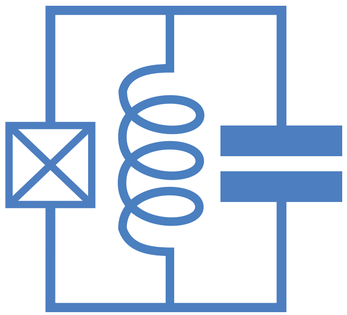
IBM Condor: 1121 qubits
(2023)

Superconducting circuits

set by nature

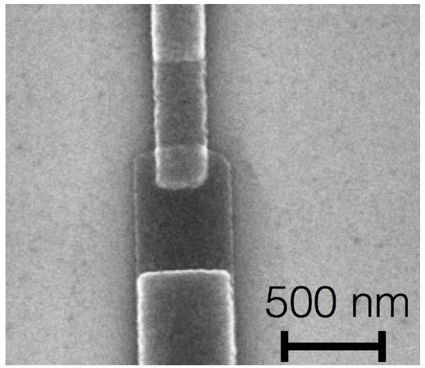


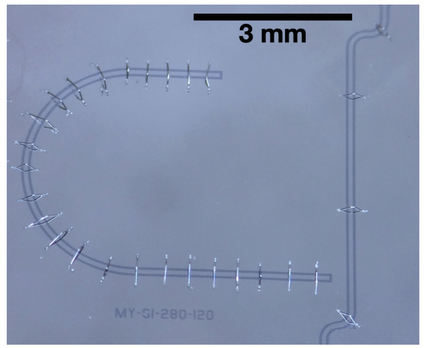
chosen by design



E_J $E_C = \frac{e^2}{2C}$

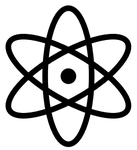
$E_L = \frac{\hbar^2}{4e^2 L}$



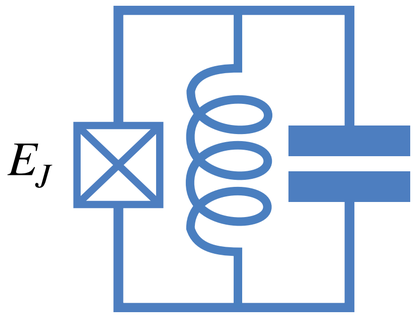


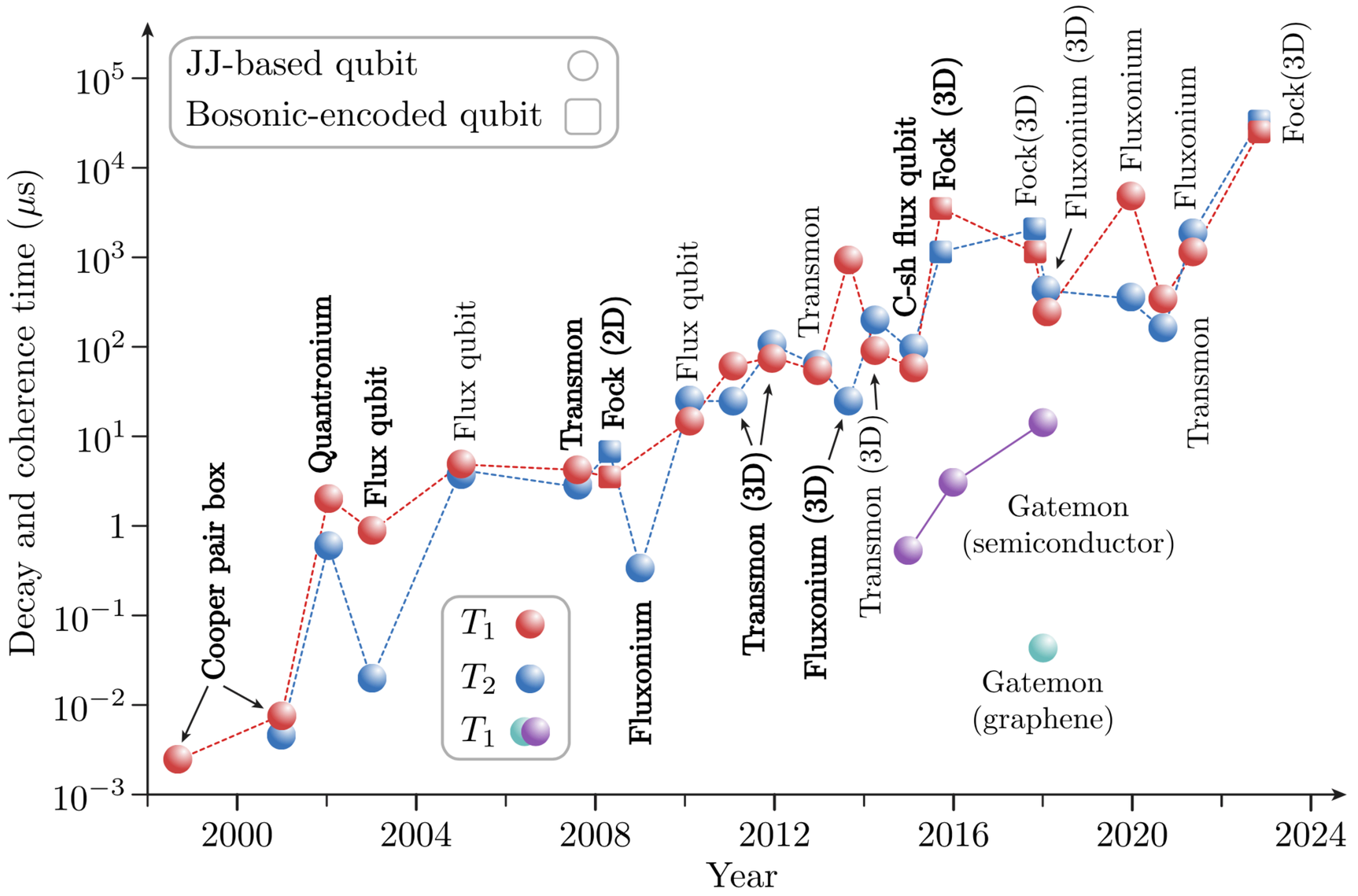
Evolution of coherence times without error correction

set by nature



chosen by design





extended version of [Kjaergaard et al., Annual Reviews of Condensed Matter Physics 2020]

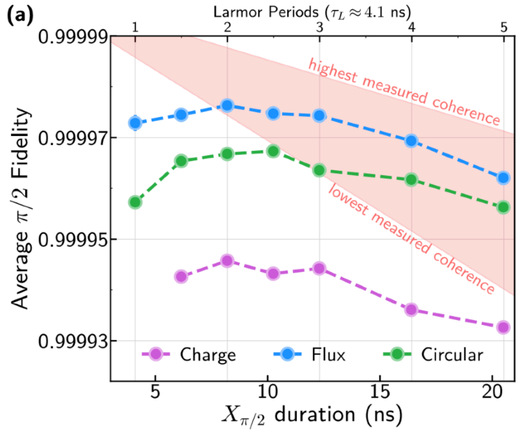
Main advantages of superconducting circuits

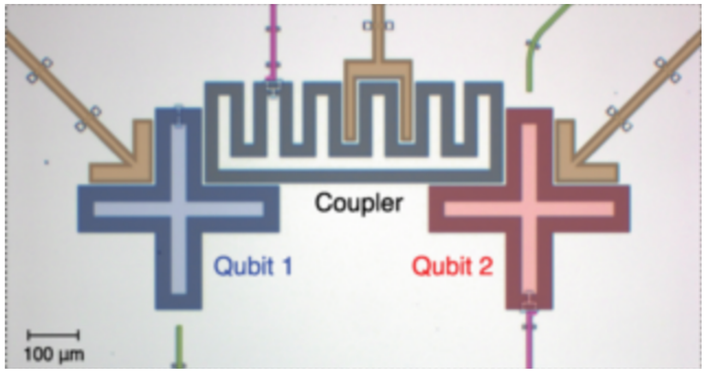
Fast gates, fast readout, fast reset (order of magnitude: 1-100 ns)

single qubit gates

2×10^{-5} errors per gate in <10 ns

[Rower et al. (MIT), arXiv:2406.08295]

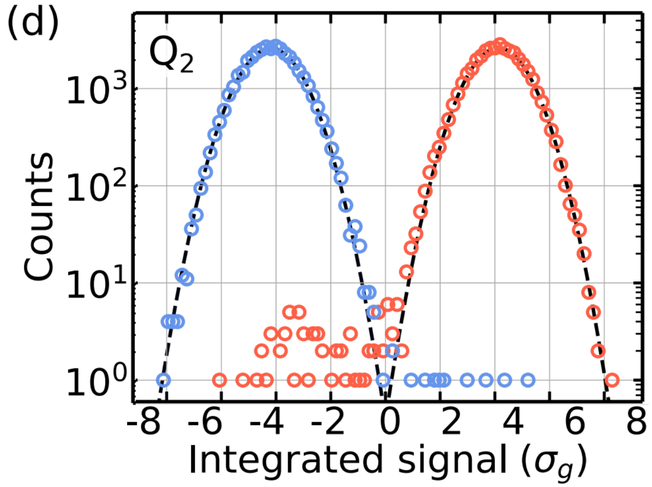




two qubit gates

1×10^{-3} errors per gate in 30 ns

[Sung et al. (MIT), PRX 2021]



readout

2×10^{-3} errors per readout in 60 ns

[Spring et al. (RIKEN), arXiv:2409.04967]

Main advantages of superconducting circuits

Fast gates, fast readout, fast reset (order of magnitude: 1-100 ns)

Fabrication process not too far from CMOS

Article

Advanced CMOS manufacturing of superconducting qubits on 300 mm wafers

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Received: 5 March 2024
Accepted: 12 August 2024

J. Van Damme[1,2], S. Massar[1], R. Acharya[1], Ts. Ivanov[1], D. Perez Lozano[1], Y. Canvel[1], M. Demarets[1,3], D. Vangoidsenhoven[1], Y. Hermans[1], J. G. Lai[1], A. M. Vadiraj[1], M. Mongillo[1], D. Wan[1], J. De Boeck[1,2], A. Potočnik[1] & K. De Greve[1,2]

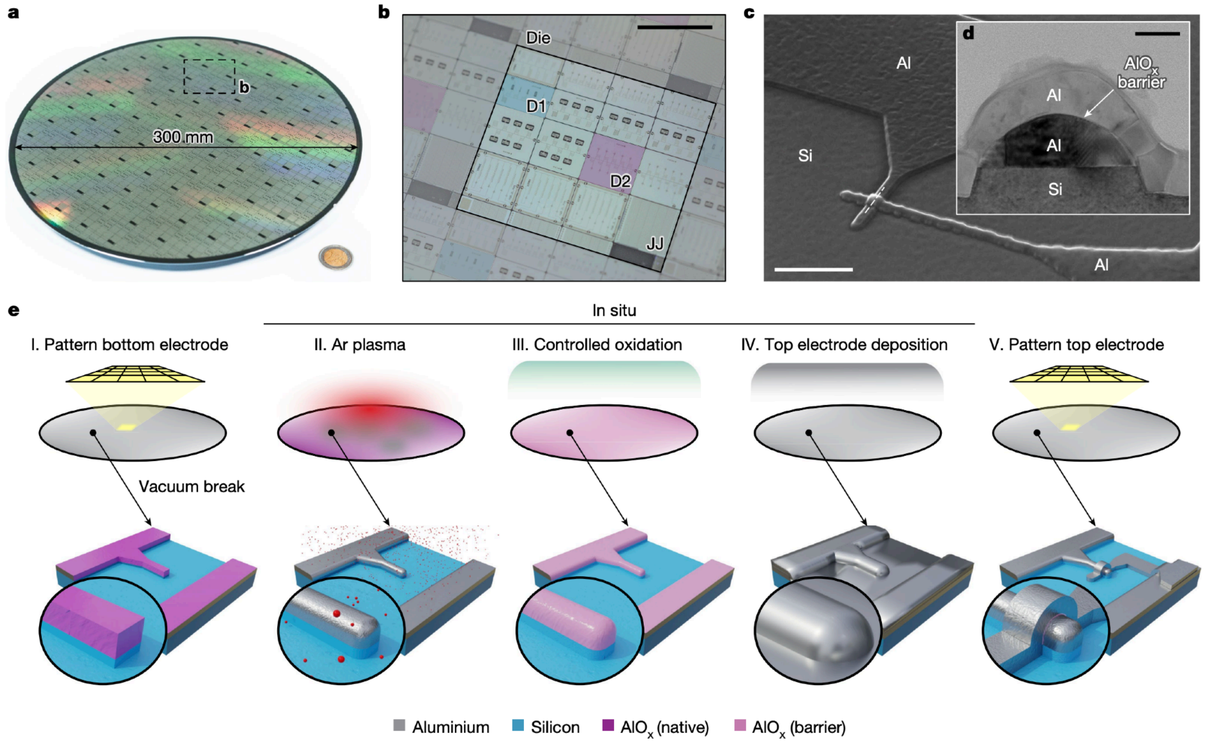

Fig. 1 | Fabrication of overlap JJ qubit. a, Photograph of the 300 mm wafer. **b**, Photograph of one die with subdie designs D1 and D2 highlighted. **c**, SEM image of an overlap JJ. **d**, Transmission electron microscopy image of a cross section of the junction (dashed line in **c**). **e**, Schematic representation of the key fabrication steps for an overlap JJ. Scale bars, 10 mm (**b**), 1 µm (**c**), 50 nm (**d**).

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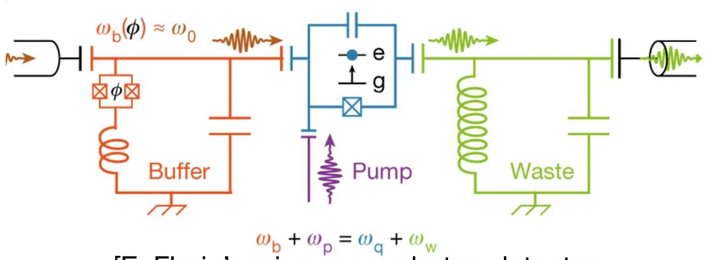

[E. Flurin's microwave photon detector PRX 2020]

Dissipation and Hamiltonian can be engineered at will

Main advantages of superconducting circuits

Fast gates, fast readout, fast reset (order of magnitude: 1-100 ns)

Fabrication process not too far from CMOS

Dissipation and Hamiltonian can be engineered at will

The qubits stay in place: no need to fight against atoms/ions escaping traps

Main advantages of superconducting circuits

Fast g set (0 ns)

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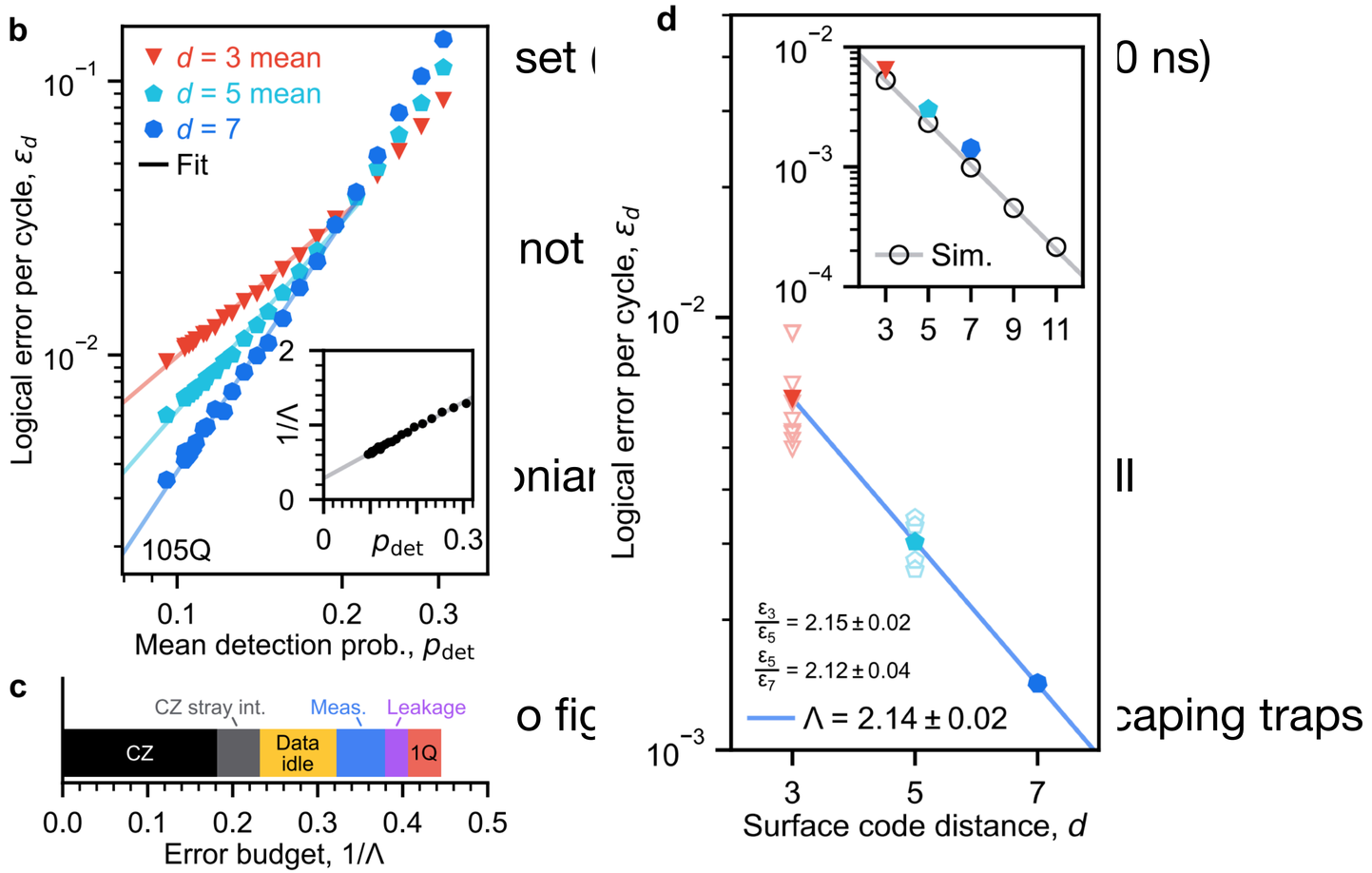

Logical qubit already demonstrated (beyond break-even and below threshold)

[Google Quantum AI, arXiv:2408.13687]

Main advantages of superconducting circuits

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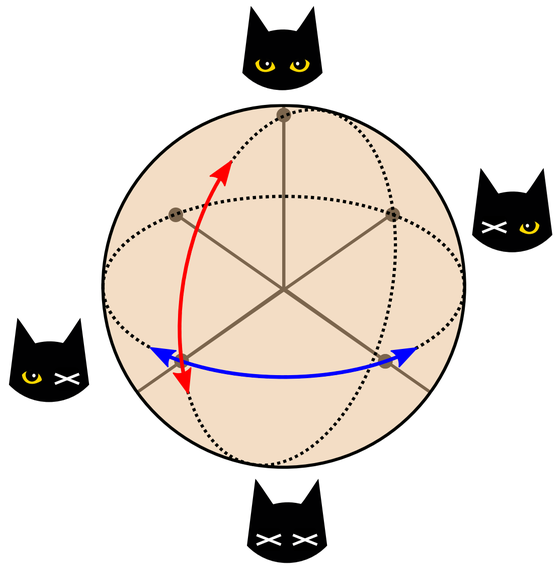

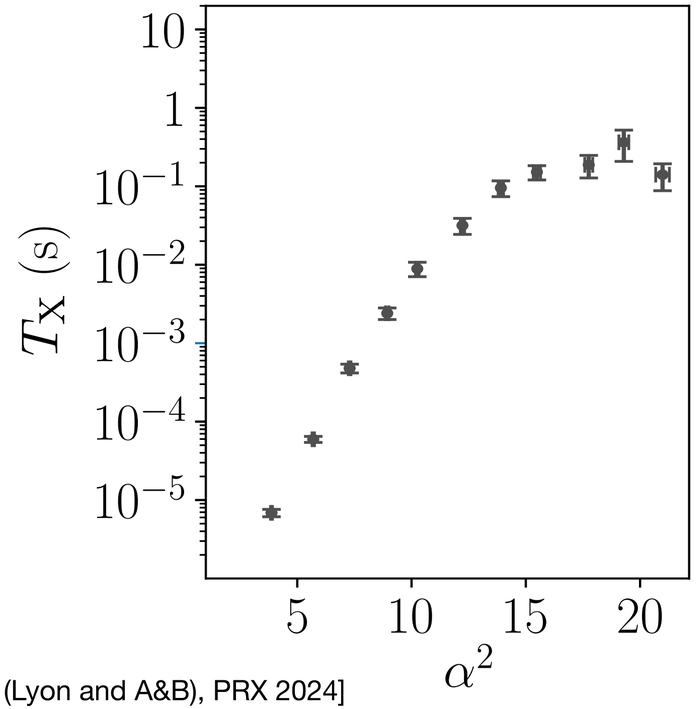

The traps

Logic shold)

[Marquet et al. (Lyon and A&B), PRX 2024]

Built-in error correction for some qubits (cat qubits, GKP, fluxonium…)

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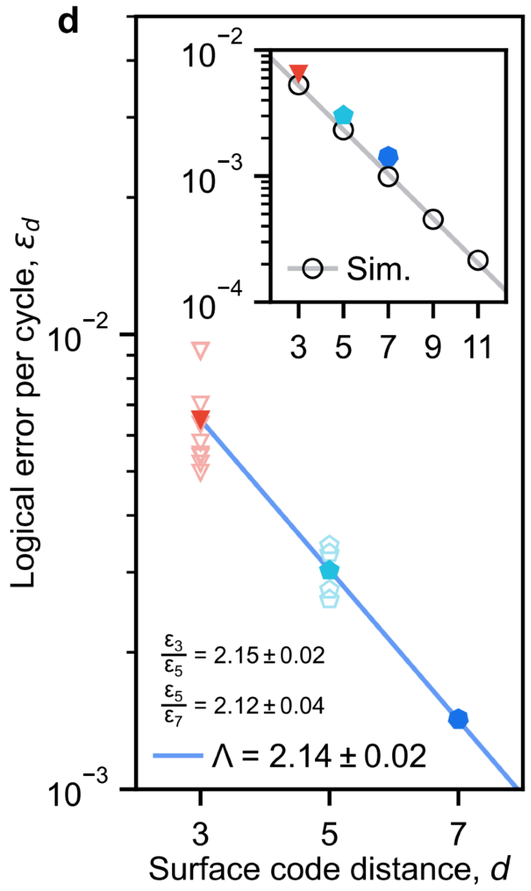
Main challenges in front of us

Reaching error rates below 10^{-6}

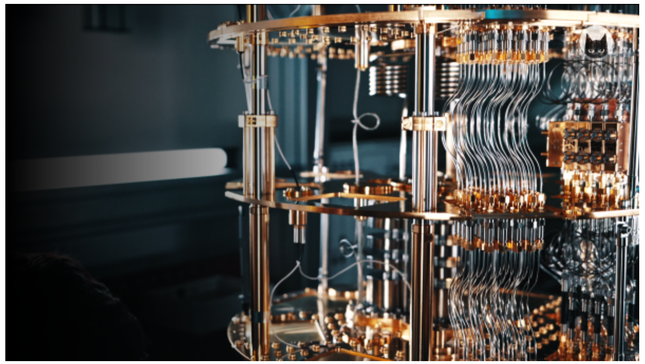


[Google Quantum AI, arXiv:2408.13687]

Main challenges in front of us

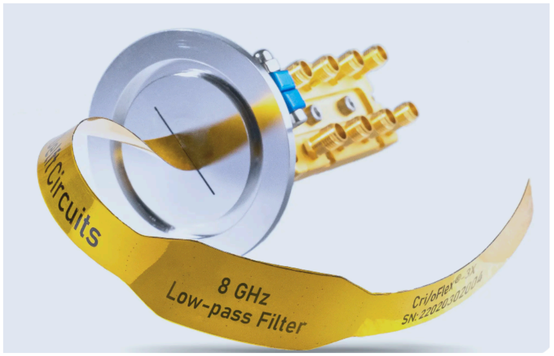
Reaching error rates below 10^{-6}

Cross-talk between control lines



[Alice&Bob]

no cross-talk but
low density

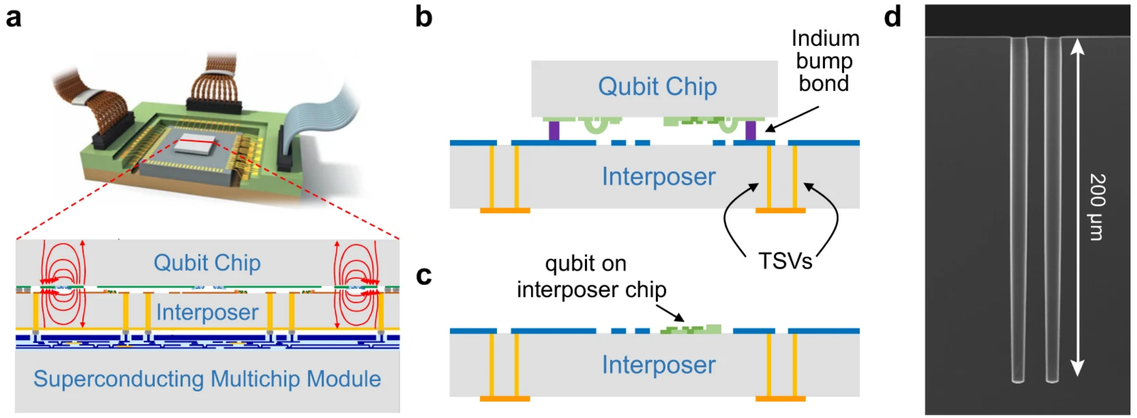


[Delft Circuits]

bad cross-talk but
high density

on chip cross-talk

bridges, flip-chip, through silicon vias…?



[D. Yost et al. (MIT), npj QI 2020]

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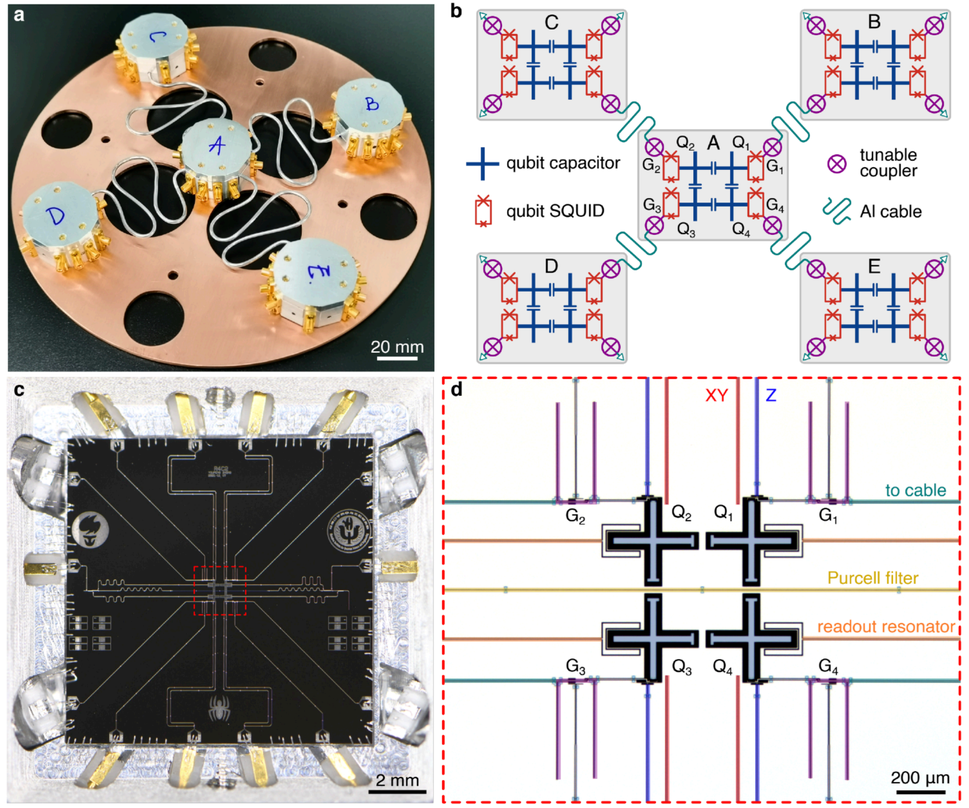
Chip to chip connectivity



1% transfer error

[Jingjing Niu et al. (Shenzhen), Nature Electronics 2023]

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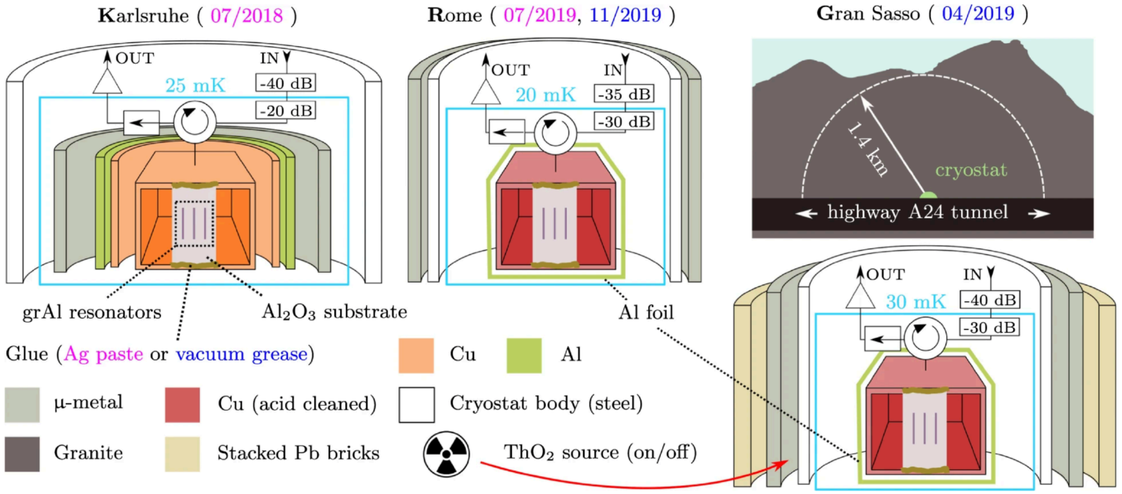
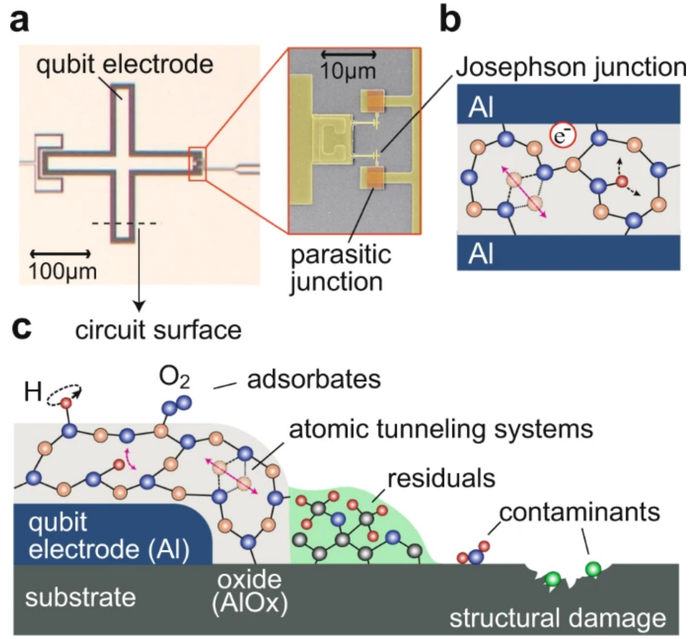
Chip to chip connectivity

Mitigating cosmic rays and parasitic Two Level Systems (TLS)





30x less bursts of quasiparticles below 1400m of rock

[Cardani et al. (KIT), Nat. Comm. 2021]

Is superconducting gap engineering enough?

[Google Quantum AI, arXiv:2402.15644]

[Lisenfeld et al. (KIT), npj QI 2019]

Main challenges in front of us

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Cross-talk between control lines

Chip to chip connectivity

Mitigating cosmic rays and parasitic Two Level Systems (TLS)

Addressing power requirements (amount and heat removal)

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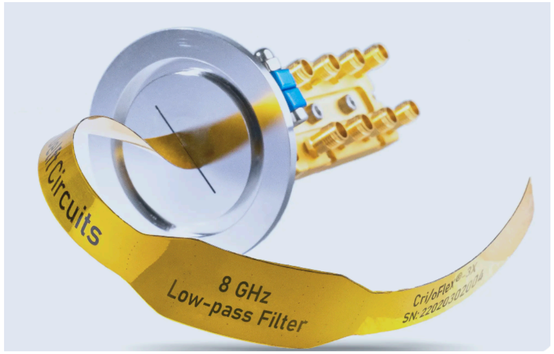
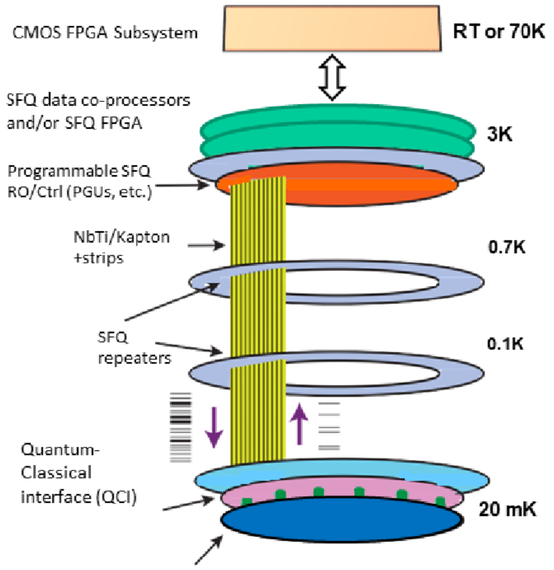
Microwave driving millions of lines at 10 mK



[Delft Circuits]



[O. Mukhanov et al. (SeeQC), IEEE IEDM 2019]

Main challenges in front of us

Reaching error rates below 10^{-6}

[KIDE fridges by Bluefors]

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[IBM]

Cooling down >10^5 logical qubits: need for new refrigerators?

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Cooling down $>10^5$ logical qubits: need for new refrigerators?

Benefitting from LDPC codes while it is hard to implement long-distance connectivity

n qubits encode k logical qubits with distance d (number of tolerable errors)

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Environmental impact

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AU SERVICE DE LA SCIENCE

QUANTERA

LPS
The Laboratory for Physical Sciences

Alice & Bob