

Algorithmic Fault Tolerance for Fast Quantum Computing

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IQuEra>

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About QuEra



Headquartered in Boston, close to Harvard and MIT.

- We build quantum computers using neutral-atoms, the most promising quantum technology.
- Deployed on the AWS cloud in November 2022.



The scientific and commercial leader in neutral-atoms



Used today to solve simulation, machine learning and optimization problems.



Recent Milestones



QuEra wins award to deploy neutral-atom computer in Japan

AIST

Working with QuEra



Machine Sales

- Purchase a QuEra computer.
- On-site installation, support, and community development.

Cloud Access

- Secure remote access.
- Mentoring and support by QuEra scientists.

Joint Development

Long-term collaborations with strategic customers to develop "killer applications"

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QuEra Quantum Alliance





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Exciting Times for Early Quantum Computing Systems





Images: Google, Quantinuum, Harvard (Bluvstein et al., Nature 2024, Maskara et al., arXiv 2023), Princeton (Holland et al., Science 2023), Berkeley

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Challenge of Large-Scale Quantum Computation

Fighting decoherence and errors is the central challenge in large-scale quantum computation



 10^{-2}

What large-scale quantum algorithms require

10-15

Error rate of encoded qubit



10-1

 10^{-3}



Image generated with DALL E

Fault Tolerance (FT) and Quantum Information

Physical qubit: single error bad!

Logical qubit: delocalized across many qubits - OK as long as not too many errors! Fault tolerance offers a deep lens into physics of quantum info:

- Fundamentally, how can we protect quantum information?
- How can we structure the qubit to be insensitive to our errors?
- We are interested in not just qubits, but *computation*
- Can we design fault tolerance for the *whole algorithm*?
- Does this have consequences for the *cost of computation*?



Space-Time Cost of Large-Scale Quantum Computation



Beverland et al., arXiv:2211.07629

Logical clock speed is usually slower by a factor of d_{i} where d is the code distance and typically around 30

Why?

Physical clock speed



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Space-Time Cost of Large-Scale Quantum Computation



Beverland et al., arXiv:2211.07629

With 100 us gate, 100 us measurement, large algorithms will take almost a year a few days

Enabled by considering fault tolerance of the entire computation, and focusing on the *classical* output of it 11



The surface code in a nutshell



[[*n*,*k*,*d*]] quantum code

- Number of physical qubit $-n = O(d^2)$
- Number of logical qubit -k = 1
- Code distance d

Data qubits (store logical information)

Ancilla qubit (measure syndrome and infer errors)

Stabilizers – commutative Pauli operators

Logical qubit – common eigenstate of +1 for all stabilizers

- Data errors can be detected by syndromes
- Syndrome errors can be detected by repeated measurements
- Logical errors are undetectable error configurations
- Logical error rates can be suppressed exponentially by increasing d

 $P_L \propto \left(\frac{p}{m}\right)^{O(d)}$

Conventional fault tolerance

- Apply logical operation
- Repeatedly measure syndrome information to detect errors
- Decode and apply correction to get correct logical information



Stabilizer was +1!

Actually, it was -1!

Hmm, maybe +1...

Repeat to be sure (*d* rounds)...



Time Cost of QEC in Lattice Surgery

Example: 2D lattice surgery with surface code (standard paradigm)



Merged logical qubit

- Introduce new stabilizers that result non-deterministic error mechanisms
- *d* rounds of SE is necessary to make error inference reliable (fault-tolerant)



See e.g. Horsman et al., NJP 2012, Fowler, Gidney, arXiv 2018

Fault-tolerant quantum computing

Different implementations of logical operations have different costs

Transversal gates

- Logical CNOT is implemented by applying pairwise physical CNOTs
- Transversal CNOT is natually fault-tolerant errors cannot spread within a patch
- Require higher-dimensional connectivity
- Natural for atom arrays efficient and highly parallel



Transversal entangling gate Shor 1996, Dennis *et al.* 2001



Error mechanisms in transversal logical gates

Transversal gates do not introduce new stabilizers – error mechanisms are deterministic



Error correlation in space

Physical errors on a logical qubit contain information about which errors occurred on other logical qubits



Error correlation in time

Syndrome measurement in future transversal logical operations can be used to validate previous syndrome measurement



Decoder should utilize the correlation between errors

Spacetime advantage of transversal logical gates



How to generalize the results to universal quantum computing?



- Fault-tolerant logical measurement with other remaining qubits
- Non-Clifford operation

M. Cain, C. Zhao et al., arXiv:2403.03272

Rethinking fault tolerance

- Quantum computing: observe classical outputs from quantum circuits Ideal distribution $P(x_1, \ldots, x_n)$
- FTQC: reliably reproduce joint logical measurement distribution of an ideal circuit, using noisy components



Transversal gates + correlated decoding + frame flipping



Algorithmic fault-tolerance for arbitrary quantum circuits with O(1) time overhead

Transversal Gates vs. Lattice Surgery

- Transversal gates with single round shows exponential error suppression
- Lattice surgery with single round is not FT and error increases with code distance







State Distillation Factory





- Distill good resource states from noisy ones, key subroutine in large-scale algorithms
- Here: Distill |Y>=S|+> (points along Y axis)

HZ*, C. Zhao* et al., arXiv:2406.17653

Magic State Distillation Factories



- Very similar structure between |S>=S|+> and |T>=T|+> magic state distillation factory
- State injection is stateagnostic, and we expect that the conclusions still hold
- |T> distillation allows universal quantum computation

patch

arowth

Magic state

Approaches to Fault Tolerance



Conventional FT

- FT individual operations
- Guarantee quantum state
 -> O(d) syndrome extraction
 (SE) rounds per operation

Transversal Algorithmic FT

- FT only when considering full algorithm
- Guarantee classical output only
- -> O(1) SE rounds per operation
- Utilize structure of initialization errors



Quantum Hardware for Transversal Algorithmic Fault Tolerance

- Wired systems (SC qubits, photonics) incur an extra cost for reconfiguring and increasing number of connections per qubit
 - Appears to be distinct requirement from longrange connectivity
- Atomic systems natively support arbitrary-degree reconfiguration
 - Native transversal logic implementation
 - 10-100x logical clock speed advantage







HZ*, C. Zhao* et al., arXiv:2406.17653; M. Cain, C. Zhao, HZ et al., arXiv:2403.03272; Bluvstein, Evered, Geim, Li, HZ et al., Nature 2024

Outlook

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Ancilla qubit resevoi

Syndrome

extraction

Logical gubit storage

Logical 1Q gate

Logical 2Q gate

ZON

Storage

Entangling zone

Readout zone

Rydbei laser



Combine with low-spaceoverhead schemes such as qLDPC codes

Hardware architecture design for neutral atom systems

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Control

Node

Contro

Control

Node

Control



Images from: Q. Xu*, P. Bonilla*,..., HZ, Nature Physics 2024; Bluvstein et al., Nature 2024; Liyanage et al., QCE 2023

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