ALICE & BOB

State of the art in hardware: Superconducting cat qubits

Jeremy Stevens

TQCI Seminar 13/11/2025

Challenges for superconducting qubits

Quantum Architecture

Efficient LDPC encoding

Tailoring algorithm to hardware

Quantum Hardware

Reaching error rates below 10^{-6}

Cross-talk between control lines

Chip to chip connectivity

Mitigating cosmic rays and TLS

Enabling technologies

Addressing power requirements

Millions of microwave lines

Cooling down > 10^5 qubits

Environmental impact

HOW DO WE PLAN TO ADRESS THESE CHALLENGES AT A&B ?

1. Use quantum architecture / hardware that **minimizes qubit count**
2. Make sure this architecture is **compatible with global effort** on enabling technologies

01
Cat qubit architecture

A hardware efficient strategy

100 logical qubits at 10^{-8}

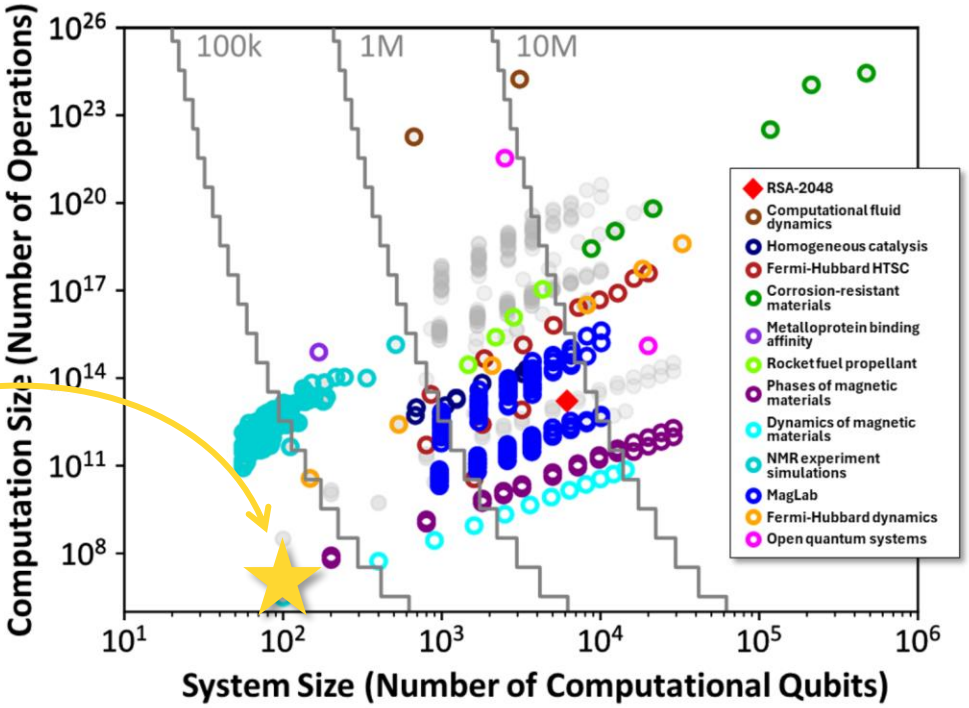
LDPC-cat codes for low-overhead quantum computing in 2D

Diego Ruiz,[1,2,*] Jérémie Guillaud,[1] Anthony Leverrier,[3] Mazyar Mirrahimi,[2] and Christophe Vuillot[4]

[1] *Alice & Bob, 49 Bd du Général Martial Valin, 75015 Paris, France*
[2] *Laboratoire de Physique de l'École Normale Supérieure, École Normale Supérieure, Centre Automatique et Systèmes, Mines Paris, Université PSL, Sorbonne Université, CNRS, Inria, 75005 Paris*
[3] *Inria Paris, France*
[4] *Université de Lorraine, CNRS, Inria, LORIA, F-54000 Nancy, France*

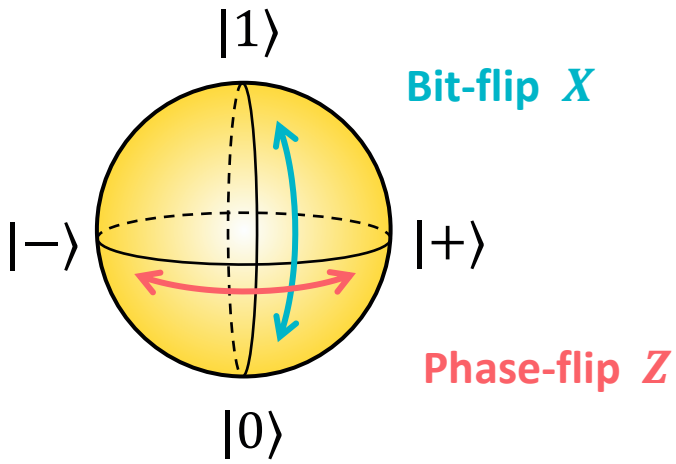
(Dated: February 7, 2024)

A 758 cat qubits memory (~1700 qubit for operations)
Assuming $F_{CX} = 98.4\%$ ($\kappa_1/\kappa_2 = 10^{-4}$)
Local connectivity 5 (4 QEC + 1 logical ops)



KEY ASSUMPTIONS

Low bit-flips
(incl. during operations)



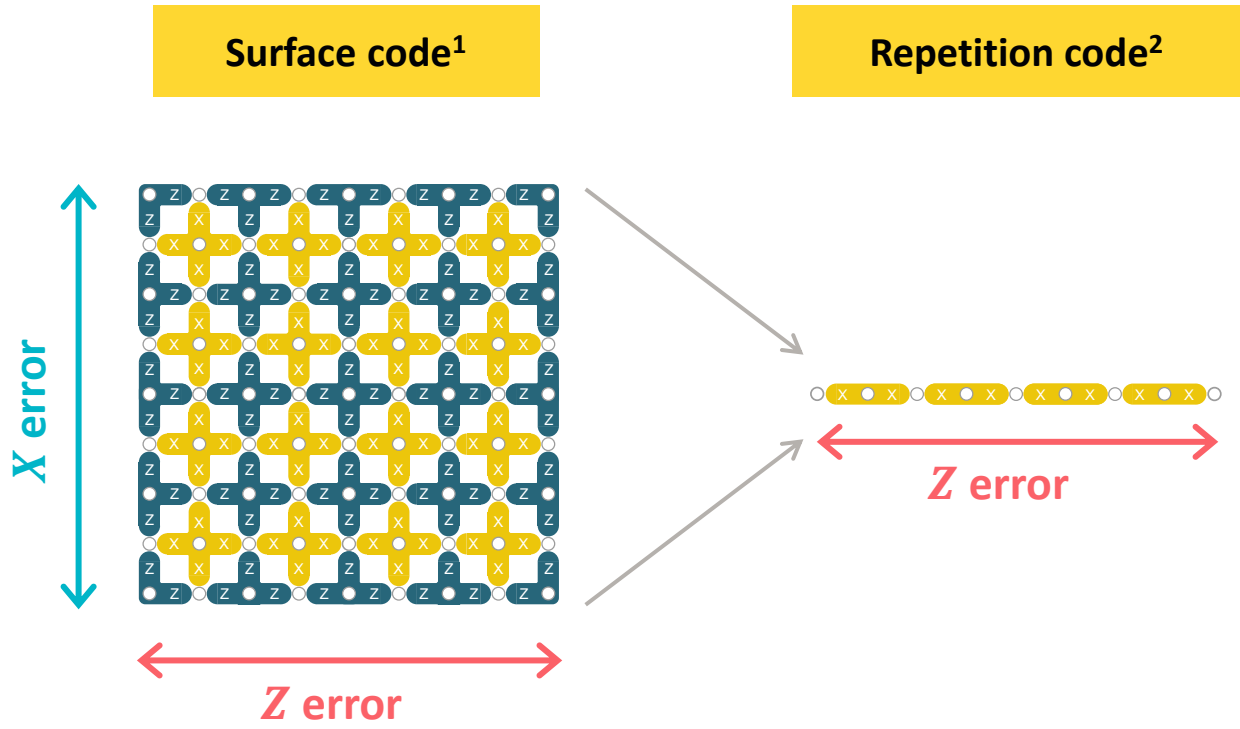
D. Ruiz et al. arXiv:2401.09541 (2024)

Using classical error correcting codes for remaining errors

What if there are “no” bit-flips ? i.e.

physical X error $\times$ # physical qubits per logical $\leq$ logical Z error

Only one error has to be corrected by the code



1. Fowler et al. PRA 86 (2012)
2. J. Guillaud and M. Mirrahimi Physical Review X 9, 10.1103 (2019)

A high threshold 1D repetition code

ENCODING

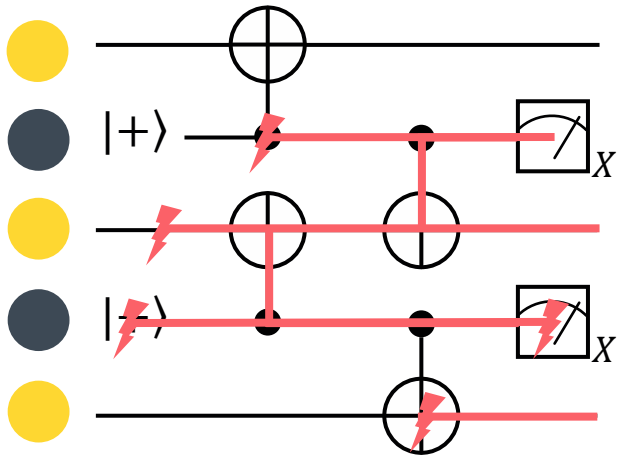
data qubit

ancilla qubit

Logical states: $|+\rangle_L = |+ + \cdots +\rangle$, $|-\rangle_L = |- - \cdots -\rangle$

Logical operators: $Z_L = \bigotimes_i Z_i$ and $X_L = X_i$

STABILIZERS $X_i X_{i+1}$



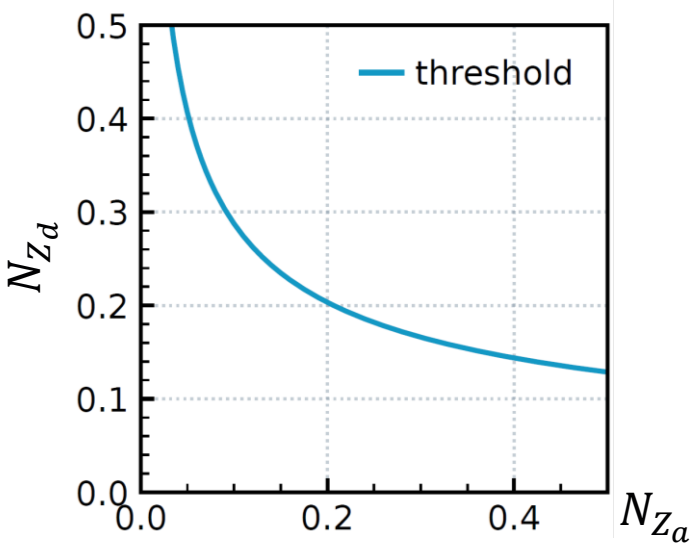
N_{Z_d} = Idle + CX

N_{Z_a} = $P_{|+\rangle}$ + CX + M_X

THRESHOLD

High threshold due to:

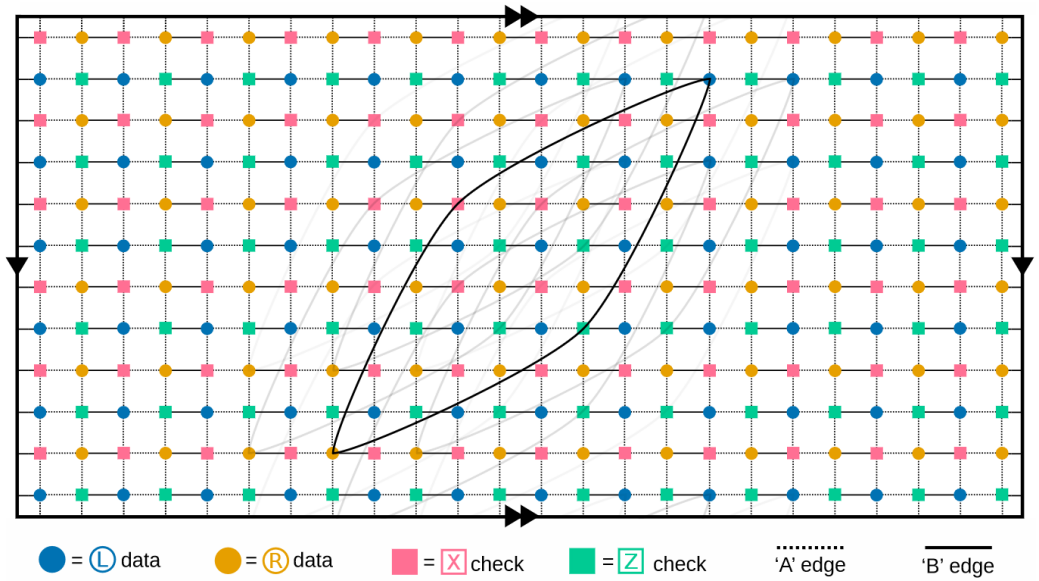
- Higher code capacity
- Low weight stabilizer



Le Régent et al. Quantum 7, 1198 (2023)

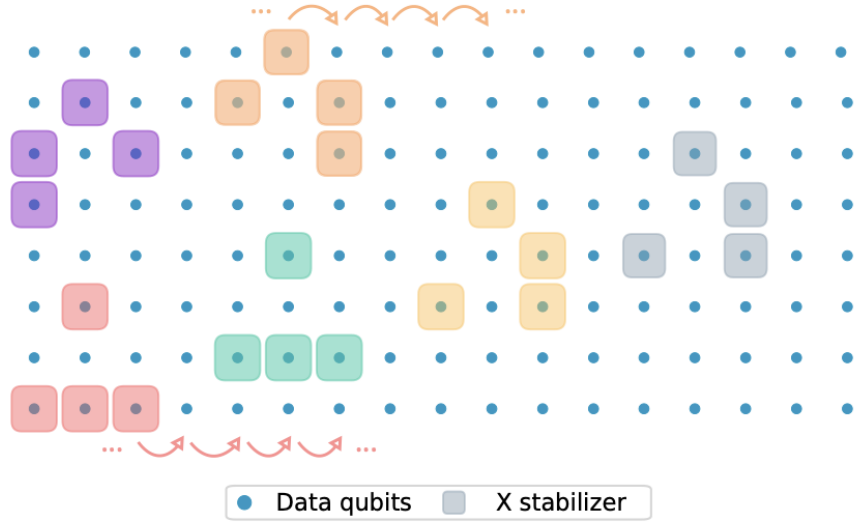
Classical LDPC code can be local in 2D

QUANTUM LDPC CODE

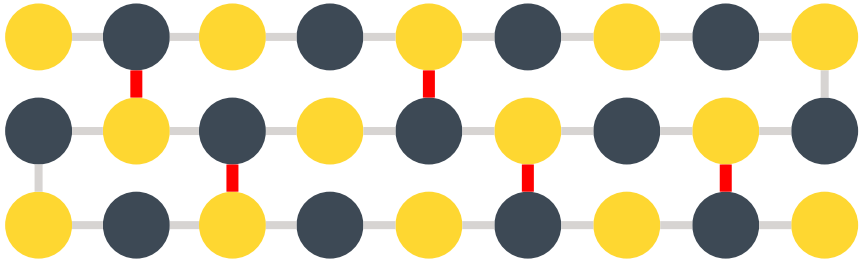


→ Requires long distance connections

CLASSICAL LDPC CODE



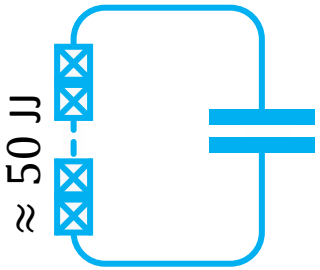
→ Becomes local since long distance in 1D become short in 2D

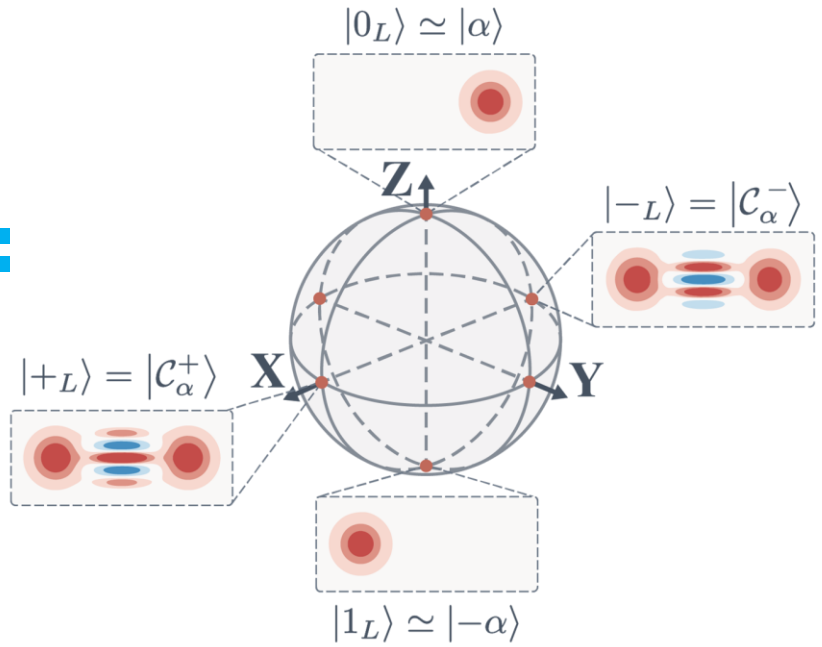


S. Bravyi et al. Nature **627**, 778–782 (2024)
D. Ruiz et al. arXiv:2401.09541 (2024)

Low bit-flip qubits

CAT QUBITS

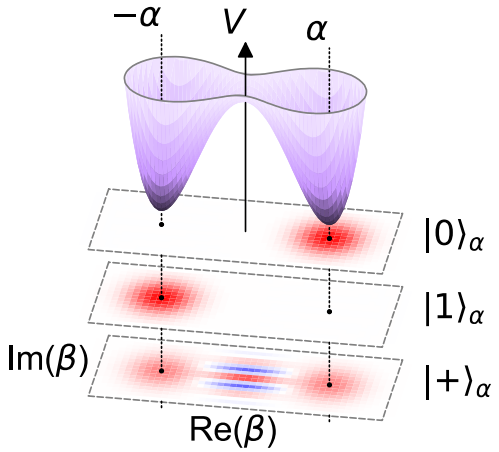


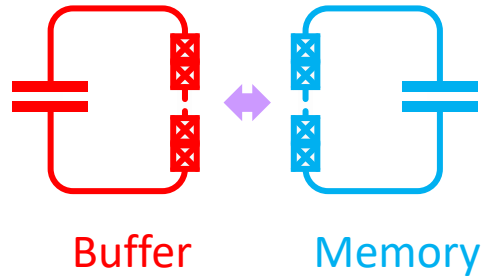


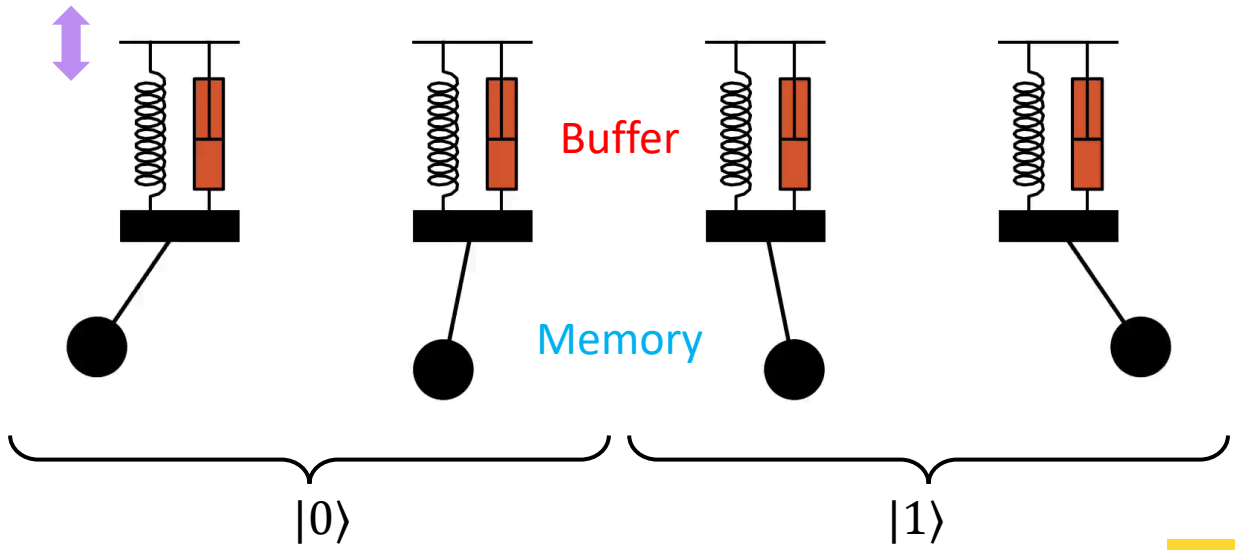
$f = 4 - 8$ GHz
$Q \approx 2 - 3 \times 10^6$
$K/2\pi \approx 100$ kHz
$|\alpha|^2 \approx 10$

Distant mesoscopic states of light makes it unlikely for local noise to create a bit-flip

TWO-PHOTON STABILIZATION



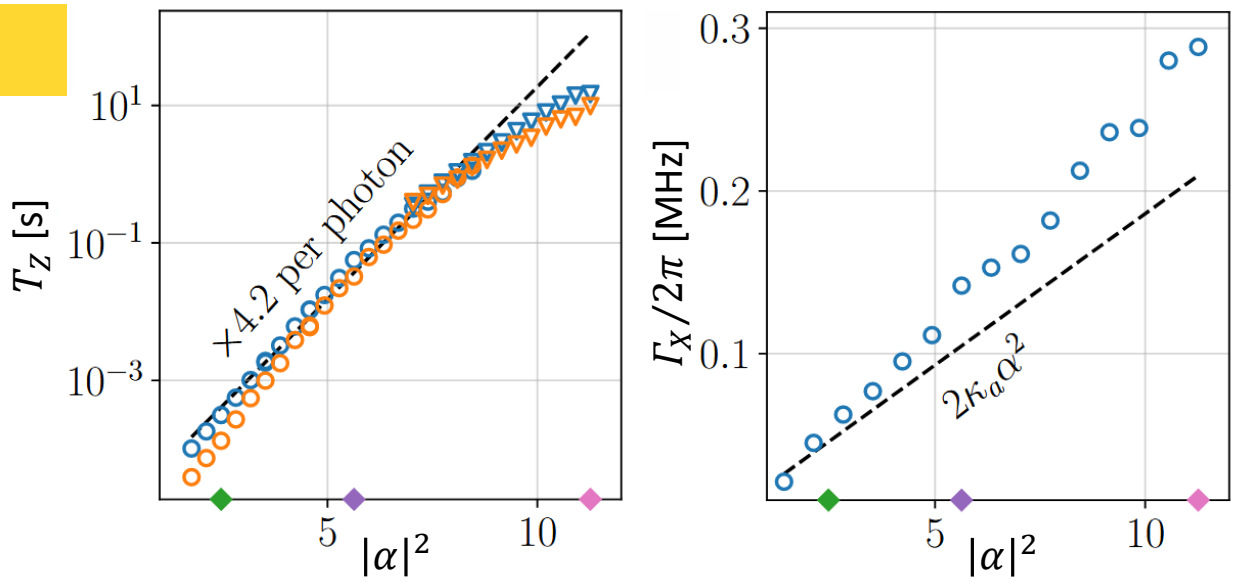




M. Mirrahimi et al. New J. Phys. 16 045014

Dissipative cat-qubits

LIFETIMES

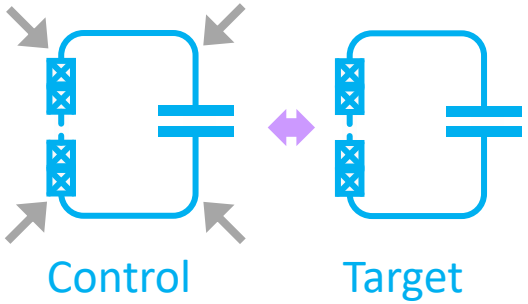


Bit-flips are suppressed exponentially →
$\Gamma_Z \propto e^{-2|\alpha|^2}$

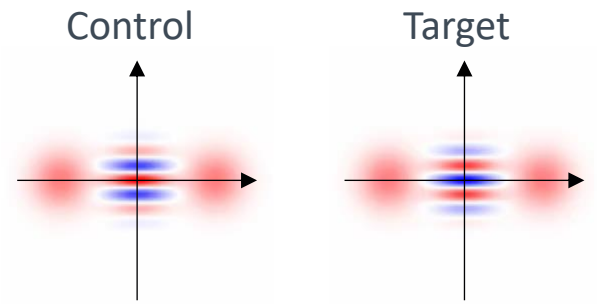
Phase-flips increase linearly
→ $\Gamma_X = 2|\alpha|^2\kappa_1$

Typ. $T_Z \approx 10$ s
$T_X = 1$ µs

BIAS PRESERVING GATES



$$H_{CX}/\hbar = g_{CX}\left(a_C + a_C^\dagger\right)a_T^\dagger a_T$$



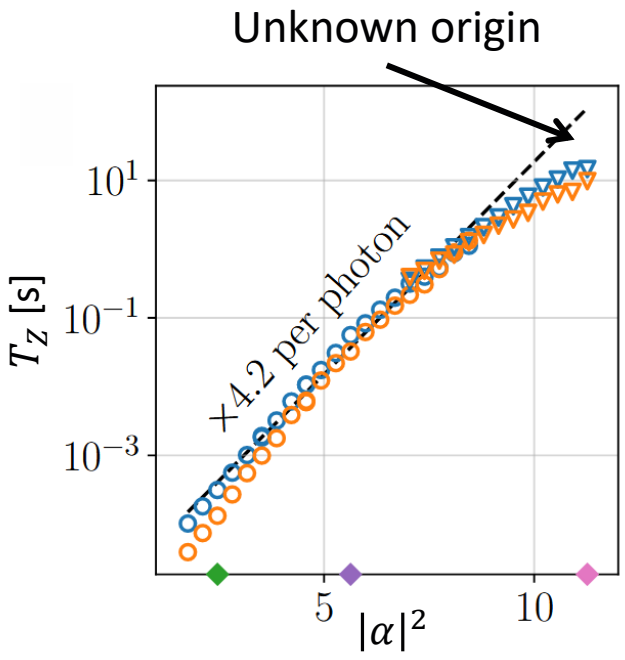
Make sure that bit-flips remain suppressed and phase-flip error are below error correction threshold

Typ. $p_Z \approx 10^{-4}$
$p_X = 15\%$

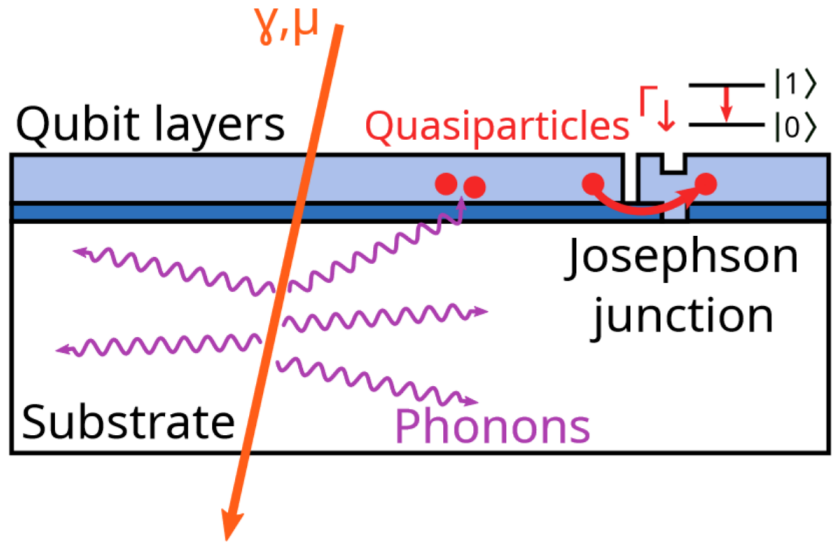
Z. Leghtas et al. Science 347, 853 (2015)
A. Marquet et al. Phys. Rev. X 14, 021019 (2024)
U. Réglade, A. Bocquet et al. Nature **629**, 778–783 (2024)

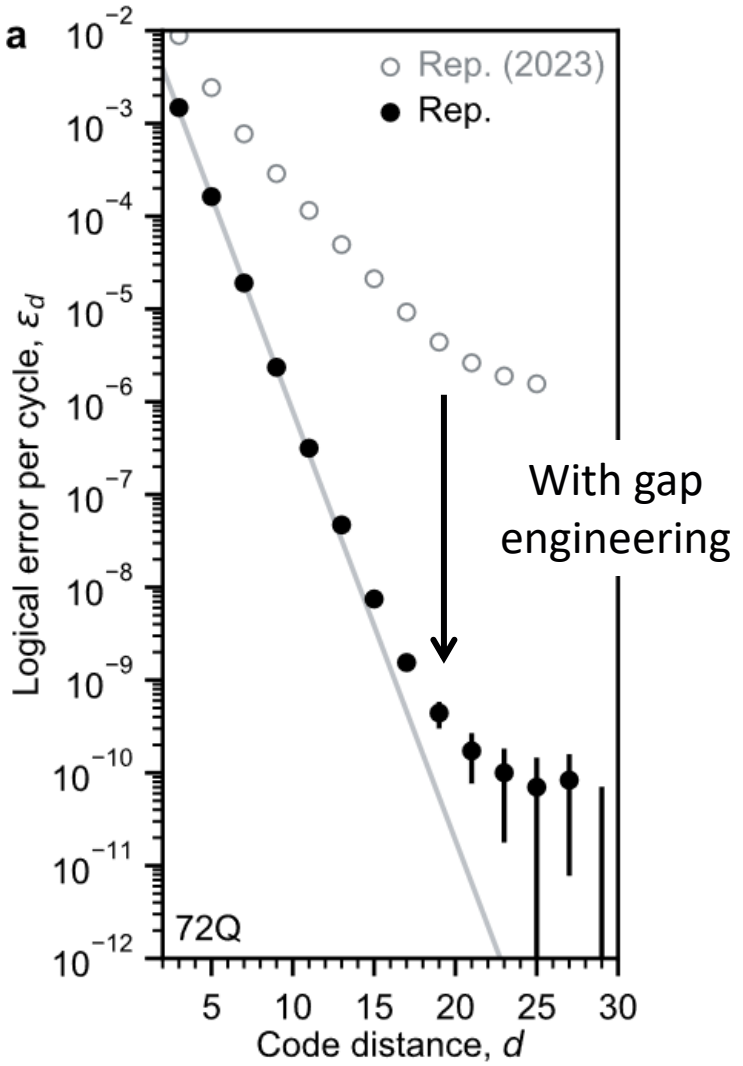
Error rates saturation

BIT-FLIP SATURATION



GOOGLE'S HYPOTHESIS & SOLUTION





Error saturation from high energy cosmic rays → JJ gap engineering [2]
Long term drifts due to spurious TLS → prediction [3]

1. U. Réglade, A. Bocquet et al. Nature **629**, 778–783 (2024)
2. M. McEwen et al. arXiv:2402.15644 (2024)
3. Google Quantum AI et al. arXiv:2408.13687 (2024)

02 Enabling technology needs

A hardware efficient strategy

100 logical qubits at 10-8

LDPC-cat codes for low-overhead quantum computing in 2D

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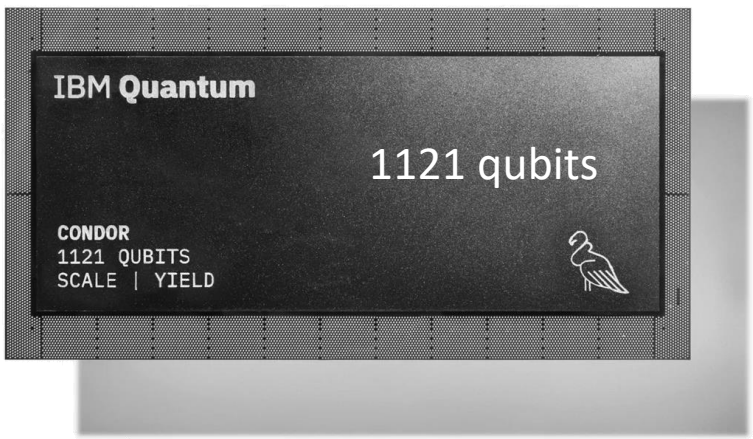
[1] *Alice & Bob, 49 Bd du Général Martial Valin, 75015 Paris, France*
[2] *Laboratoire de Physique de l'École Normale Supérieure, École Normale Supérieure, Centre Automatique et Systèmes, Mines Paris, Université PSL, Sorbonne Université, CNRS, Inria, 75005 Paris*
[3] *Inria Paris, France*
[4] *Université de Lorraine, CNRS, Inria, LORIA, F-54000 Nancy, France*

(Dated: February 7, 2024)

1700 cat qubits

Close to the largest super-conducting qubit chip by IBM



Estimated **200-fold qubit count reduction** compared to standard superconducting qubits with similar physical assumptions.

200 times less hardware should reduce:
- power required
- microwave lines
- qubits to cooldown

TAYLORING ALGORITHMS

- FTQC optimization is vastly different from NISQ.
- Resource estimation is done by assuming logical gates happen one after the other.
  → Dedicated line of work, for compilation and architecture optimization.

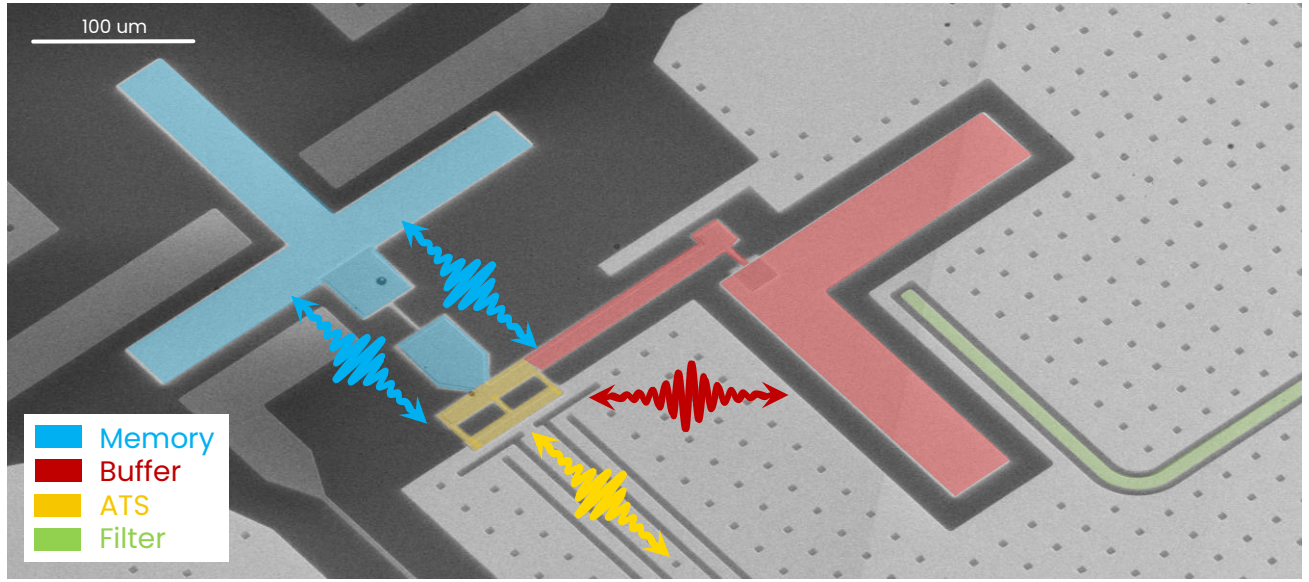
É. Gouzien, et al. Phys. Rev. Lett. 131, 040602 (2023)
D. Ruiz et al. arXiv:2401.09541 (2024)

Superconducting qubit fabrication bottleneck

IMPLEMENTATION

Uses standard superconducting qubit components:

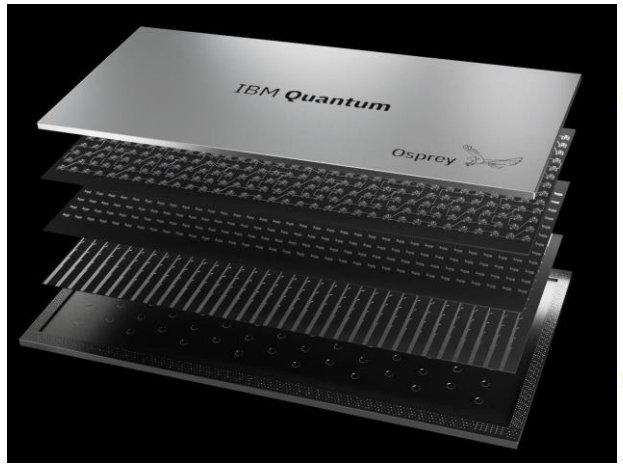
- planar fabrication techniques
- Sapphire or silicon substrate
- Aluminium Josephson junctions
- ...



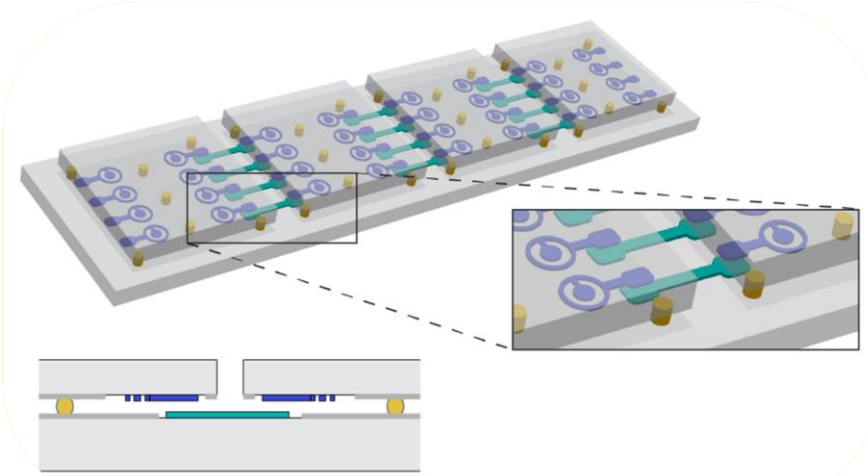
LARGE SCALE CHIPS

Requires:

- Multi-layer chips prevents routing issues
- Chiplet strategy[1] prevents chip yield limitation



Multi-layer



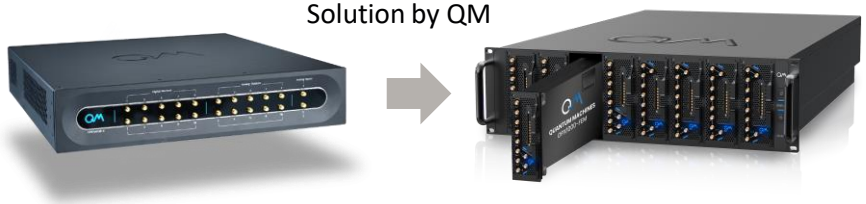
Chiplets

1. A. Gold et al. npj Quantum Inf 7, 142 (2021)

Beyond 100 logical qubits: hypotheses

CONTROL ELECTRONICS

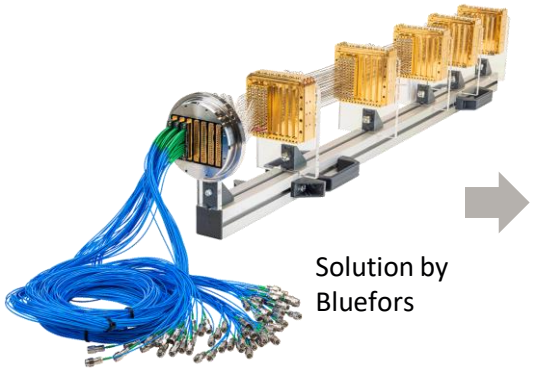
Solution by QM



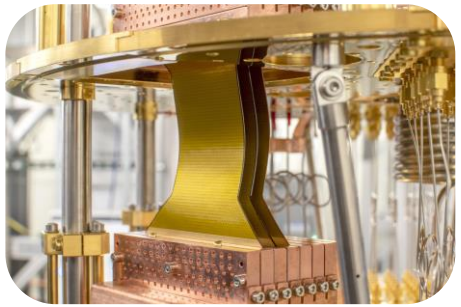
Exploring:

- cryogenic control electronics
- SFQ electronics (e.g. SeeQC)

INPUT/OUTPUT

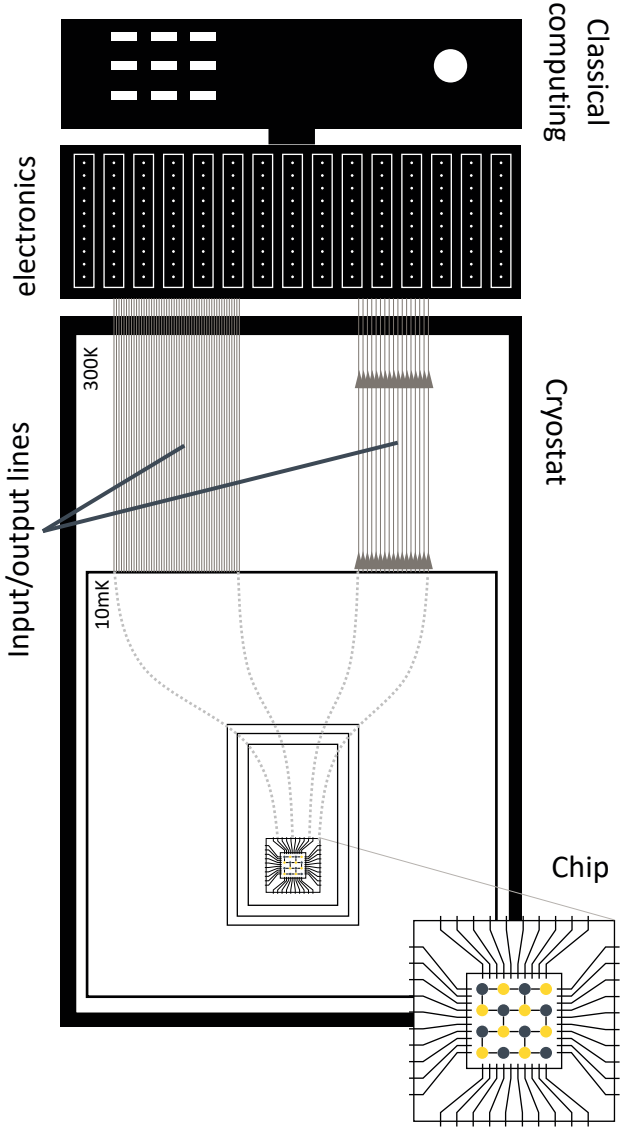


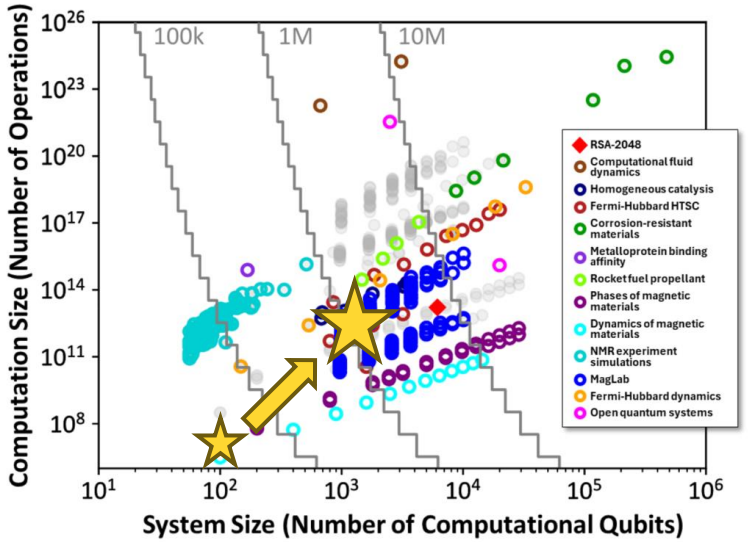
Solution by Bluefors



Solution by IBM

High density / Low thermal conductivity





CRYOSTAT

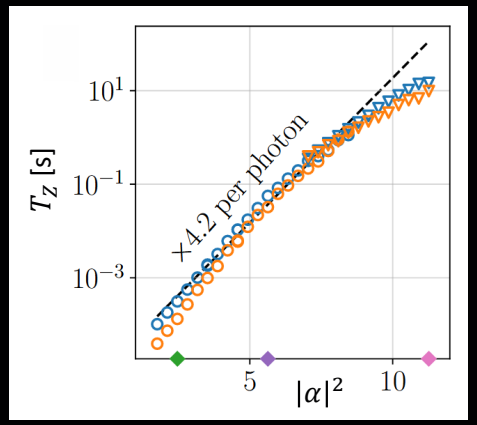
Larger monolithic cryogenic system

Target no room temperature connexions

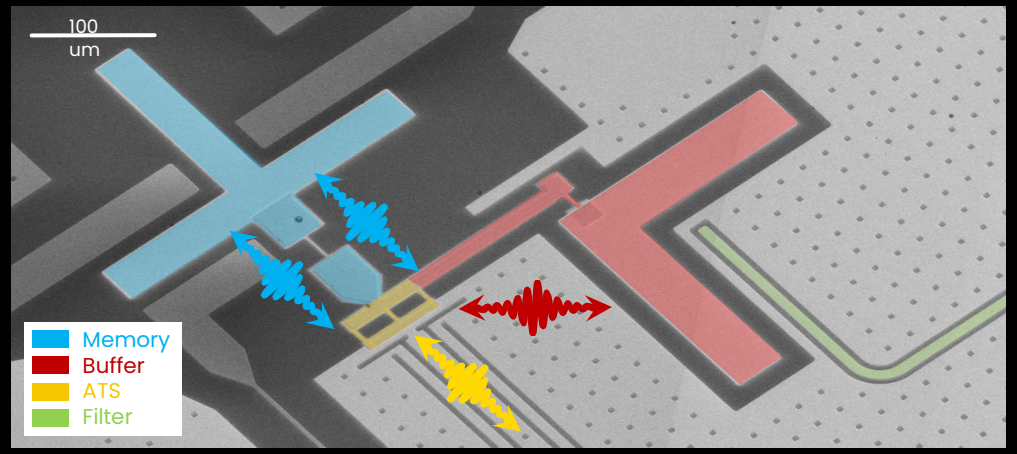
Solution by Bluefors

To summarize

1. If there are no bit-flips QEC becomes more resource efficient
   → Alice & Bob is working on demonstrating this assumption



2. Cat qubit have similar needs as the other superconducting platforms
   → mutualizing the development efforts are possible



THANK YOU FOR YOUR ATTENTION !

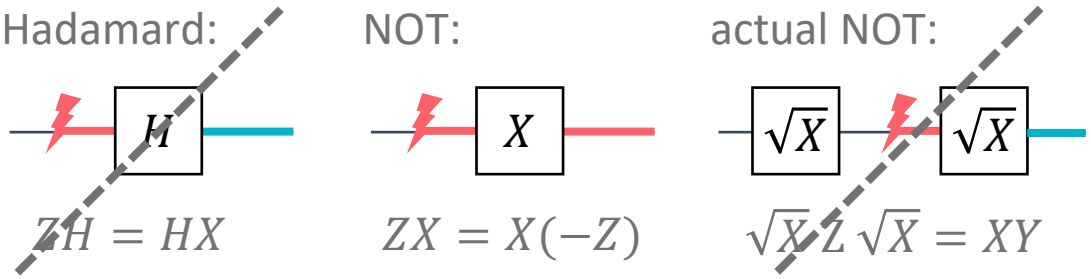
Founded in 2020
Raised 30 M€
100+ people (40+ PhD)

Based in Paris 15e
Open positions (interns, PhDs, permanents)

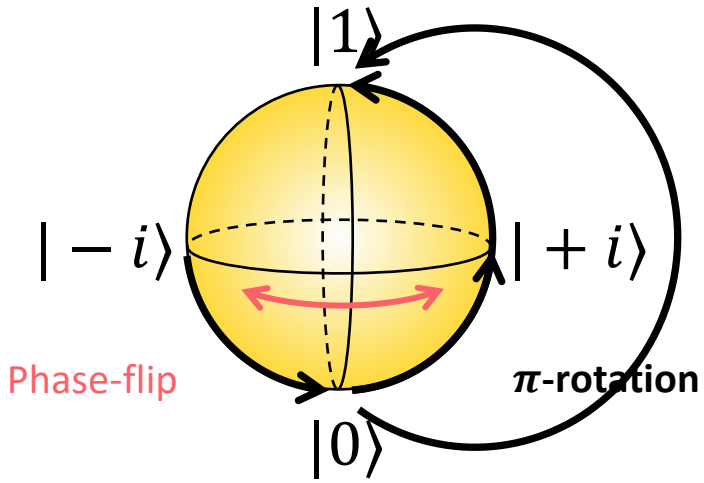
03
Maintaining low bit-flips during operations

Leveraging a biased-noise qubit

Hadamard: NOT: actual NOT:

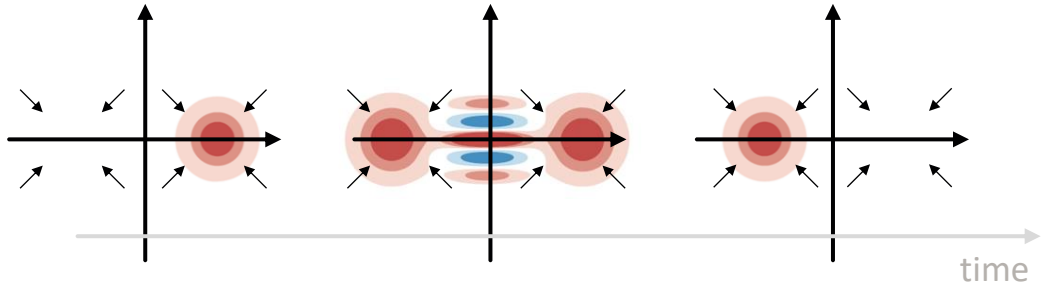


X gate should convert $|0\rangle$ into $|1\rangle$

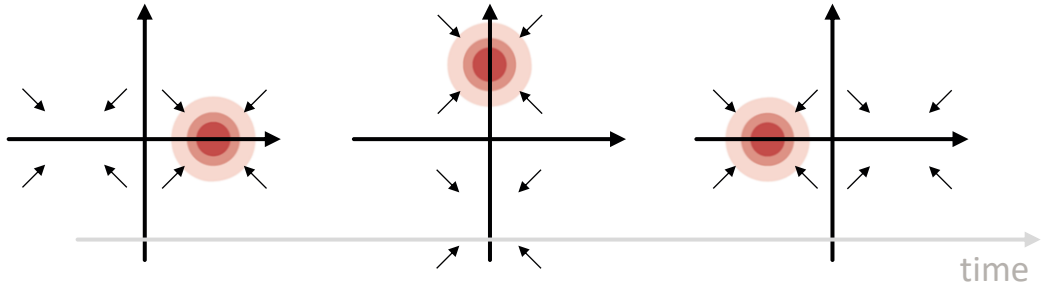


Passing through a “fragile” state converts a phase-flip into a bit-flip

Noise depolarizing X gate implementation



Bias-preserving X gate implementation



All physical gates should be bias preserving

J. Guillaud and M. Mirrahimi Physical Review X 9, 10.1103(2019)
S. Puri et al., Science Advances 6, eaay5901 (2020)

Preserving bit-flips in the 1D repetition code

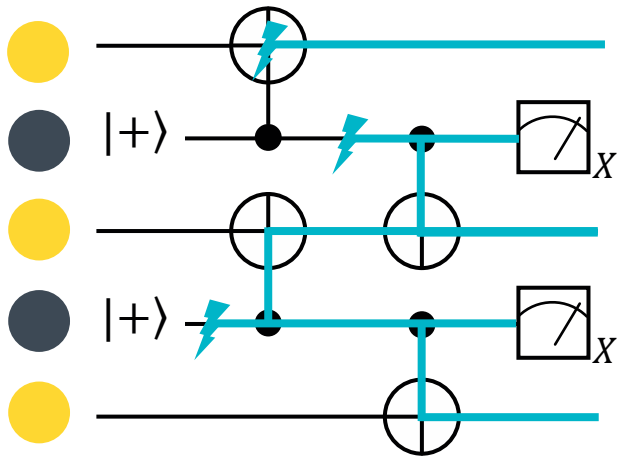
ENCODING

data qubit

ancilla qubit

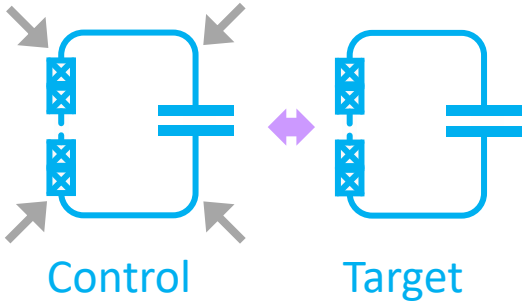
Logical states: $|+\rangle_L = |+ + \cdots +\rangle$, $|-\rangle_L = |- - \cdots -\rangle$
Logical operators: $Z_L = \bigotimes_i Z_i$ and $X_L = X_i$

STABILIZERS $X_i X_{i+1}$

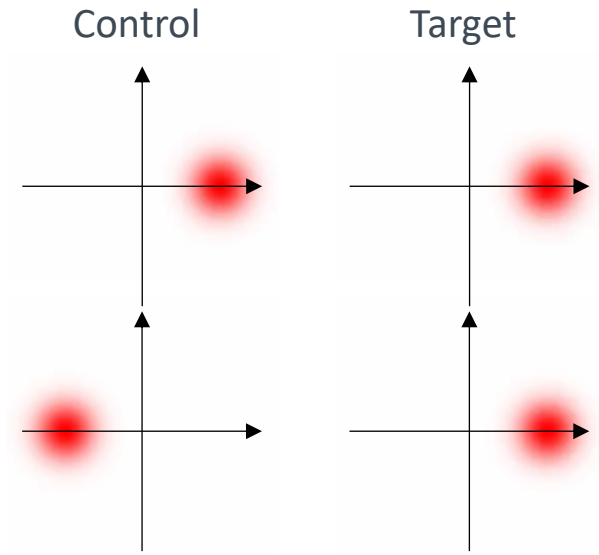


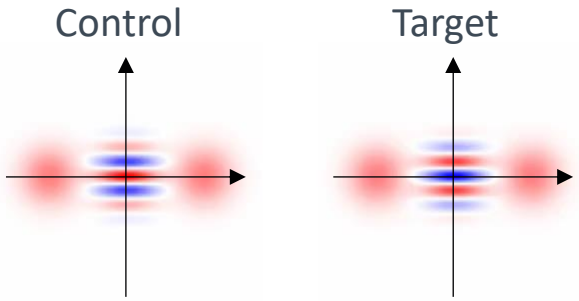
- CNOT should not create data bit-flips.
- Ancilla bit-flip errors propagate to the data
- Only between the CNOT gates

CNOT PRINCIPLE



$$H_{CX}/\hbar = g_{CX}\left(a_C + a_C^\dagger\right)a_T^\dagger a_T$$

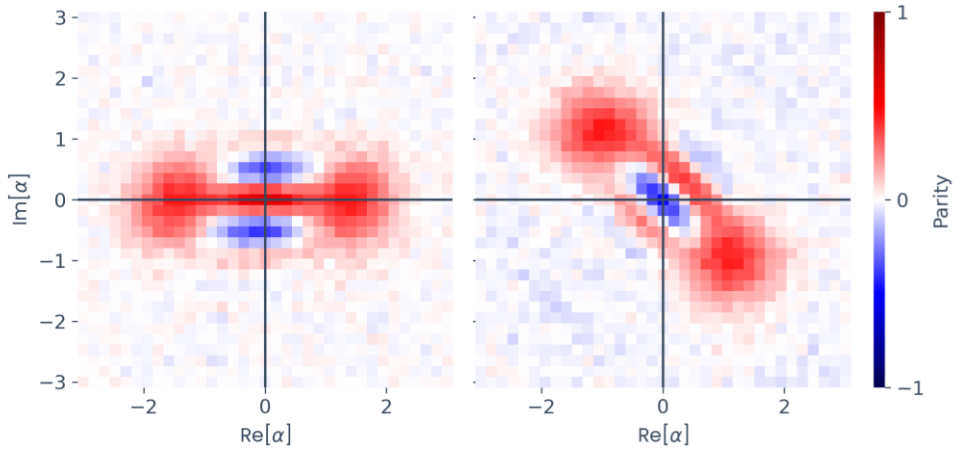




Status of our CX development progress

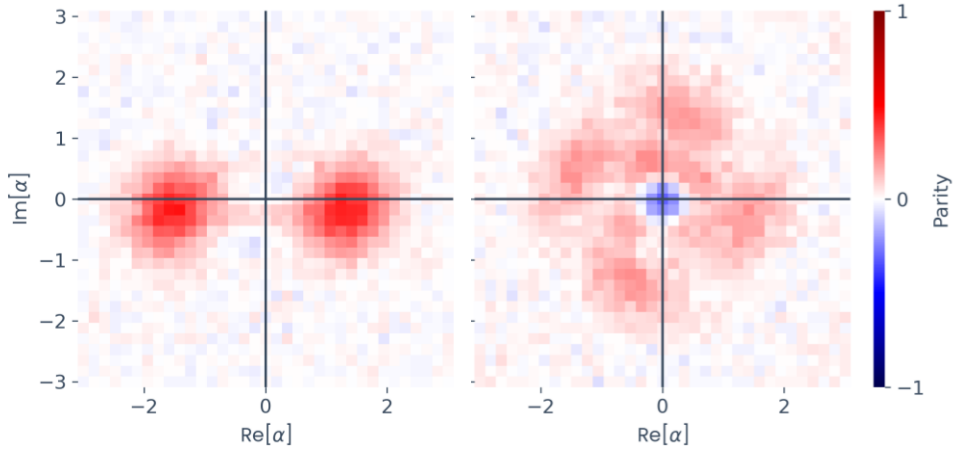
AT START

$(|\alpha\rangle + |-\alpha\rangle)\otimes(|\alpha\rangle - |-\alpha\rangle)$



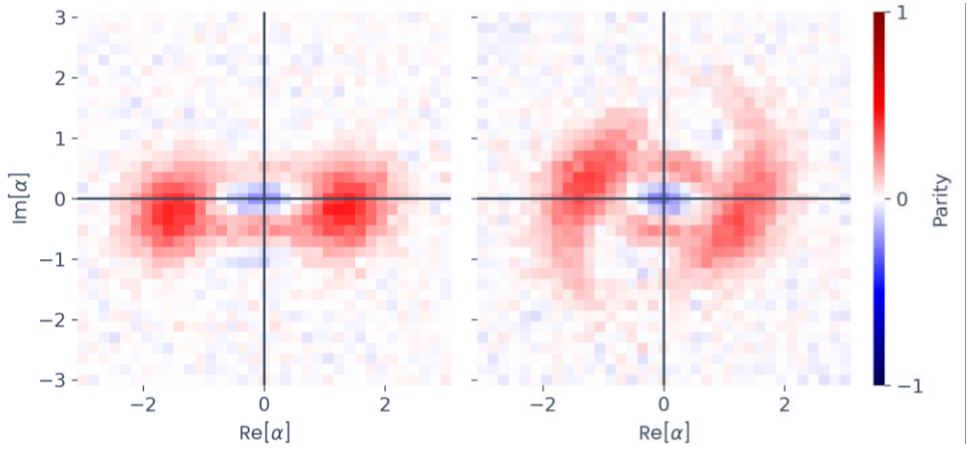
DURING CX

$|\alpha\rangle\otimes(|i\alpha\rangle - |-i\alpha\rangle) + |-\alpha\rangle\otimes(|\alpha\rangle - |-\alpha\rangle)$



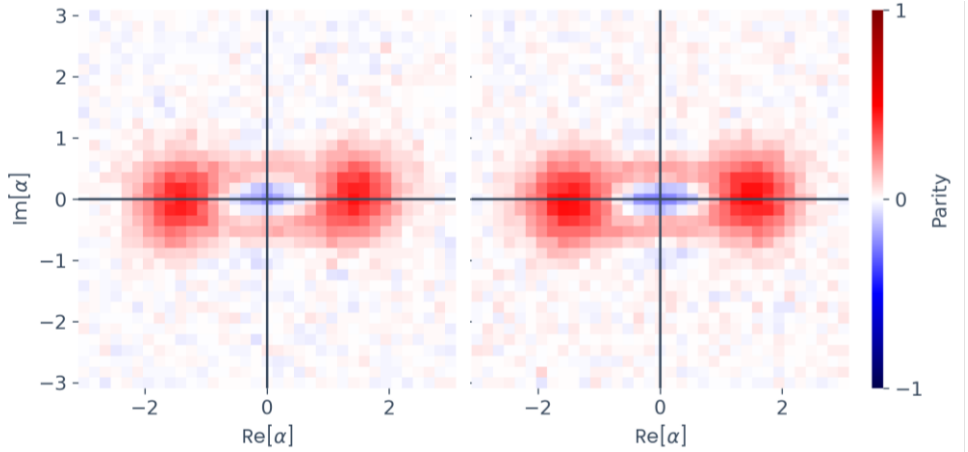
AFTER CX

$(|\alpha\rangle - |-\alpha\rangle)\otimes(|\alpha\rangle - |-\alpha\rangle)$



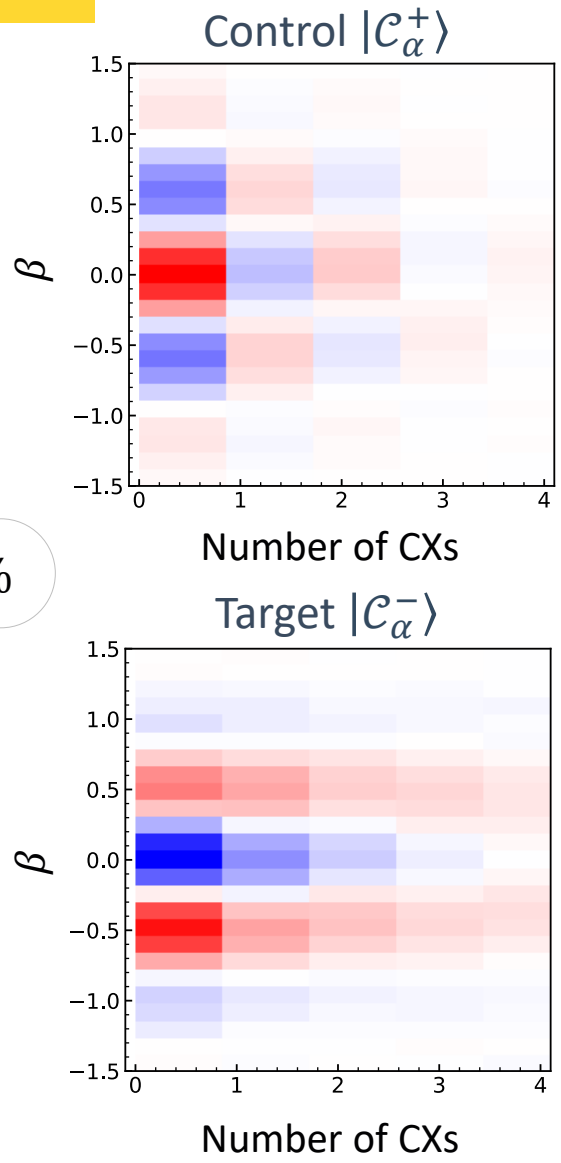
AFTER RESTAB.

$(|\alpha\rangle - |-\alpha\rangle)\otimes(|\alpha\rangle - |-\alpha\rangle)$



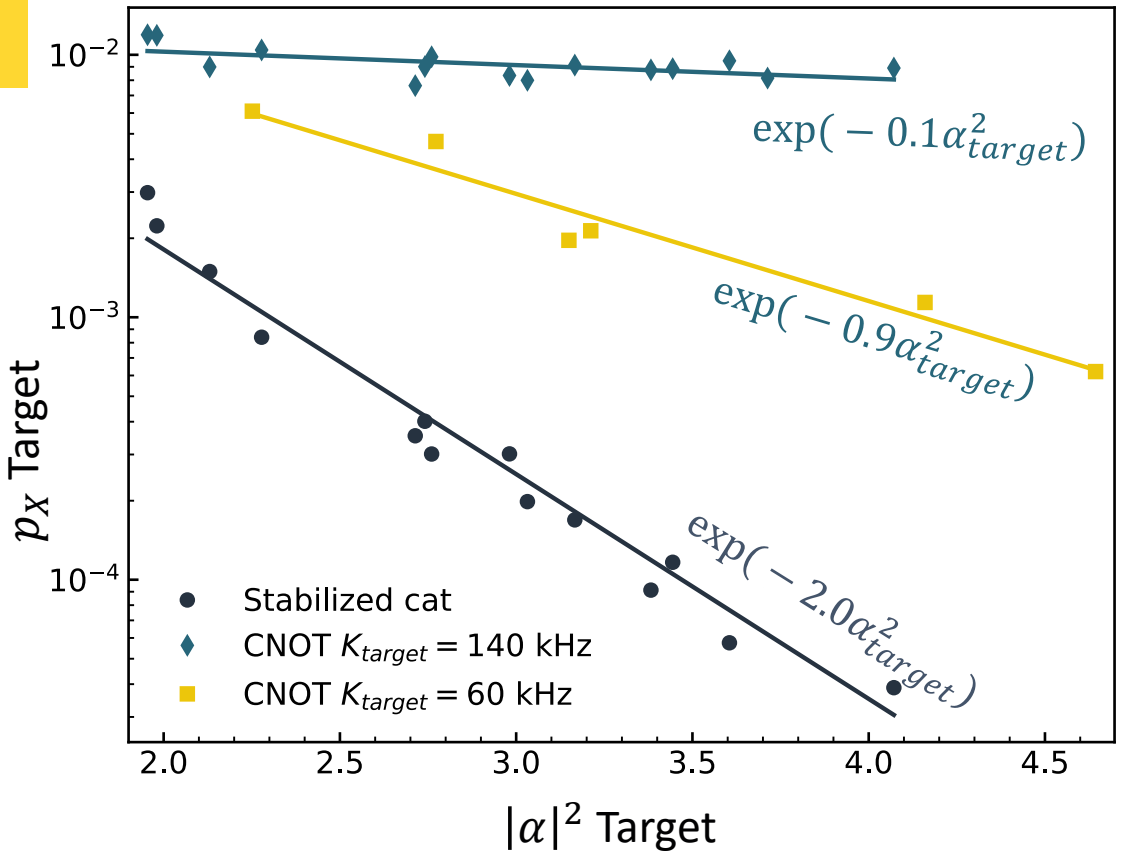
Characterizing the CX gate

Z ERRORS



$p_Z \approx 15\ \%$

X ERRORS

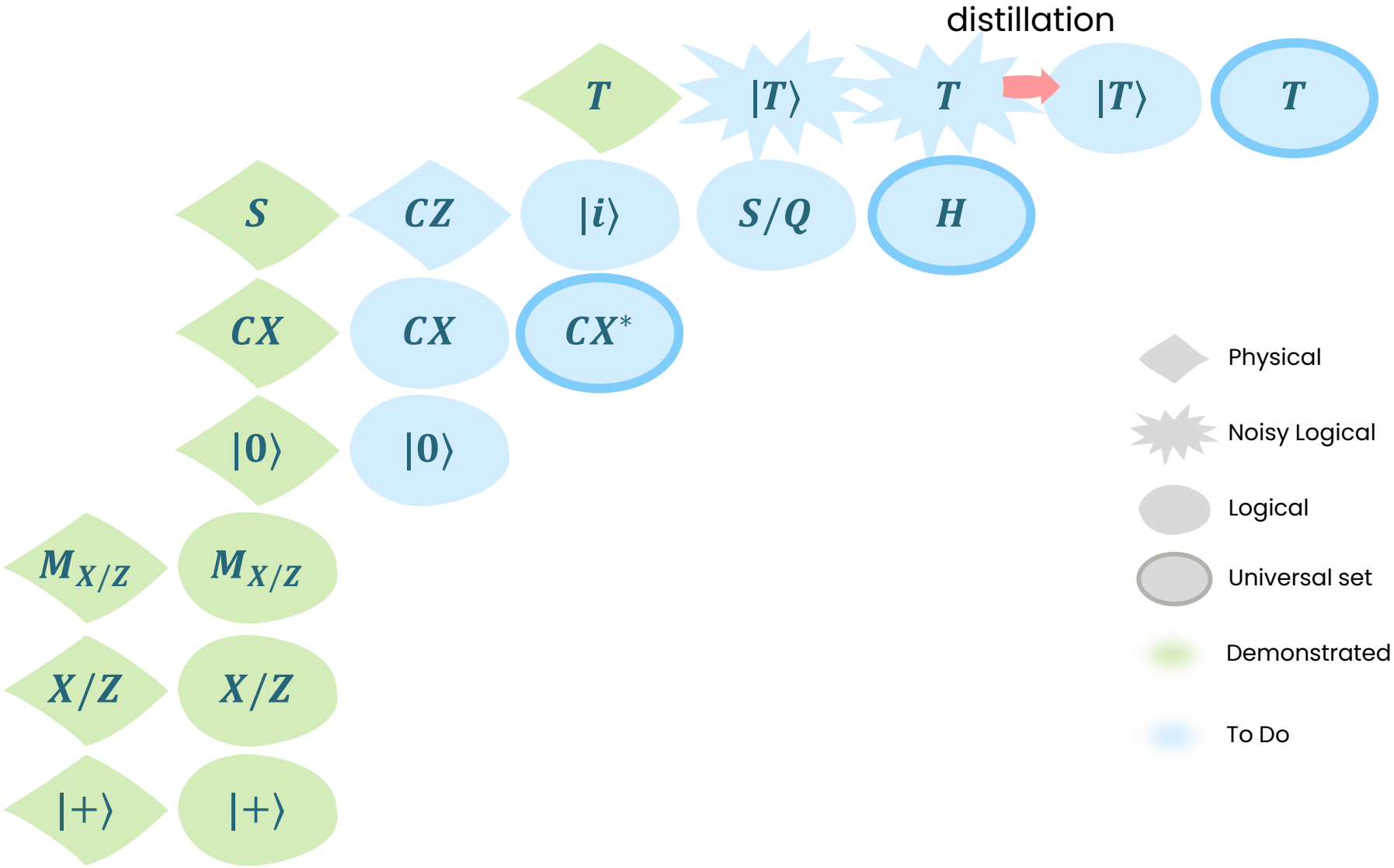


Limited by leakage when stabilization off

- Reduce Kerr and dephasing
- Engineer conditional target dissipation

J. Guillaud and M. Mirrahimi Physical Review X 9, 10.1103 (2019)

Universal logical set from bias-preserving operations



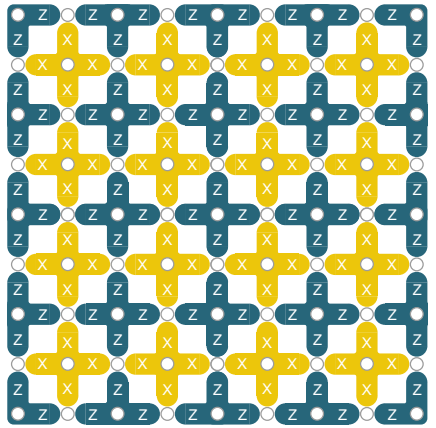
J. Guillaud and M. Mirrahimi Physical Review X 9, 10.1103 (2019)
D. Litinski Quantum 3, 205 (2019)
C. Gidney, A. G. Fowler Quantum 3, 135 (2019)

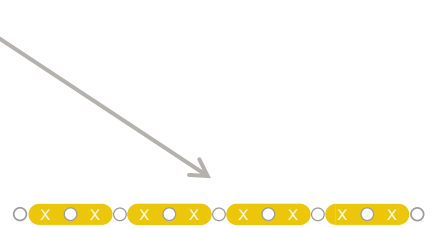
Origin of Hardware efficiency

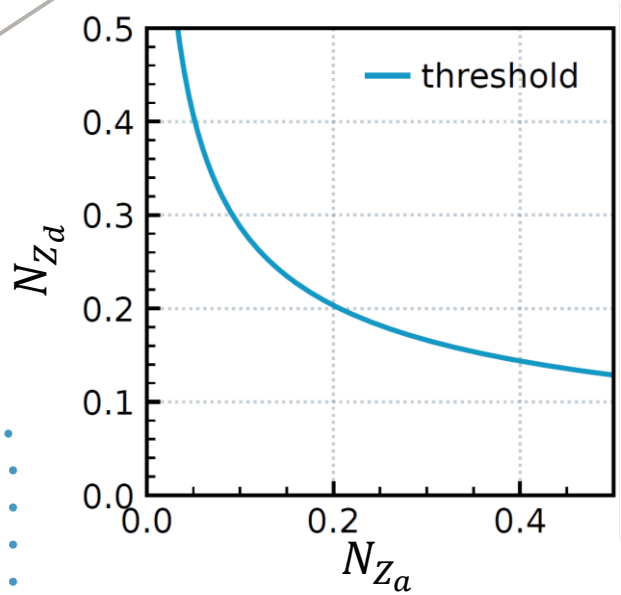
1. Classical codes are sufficient

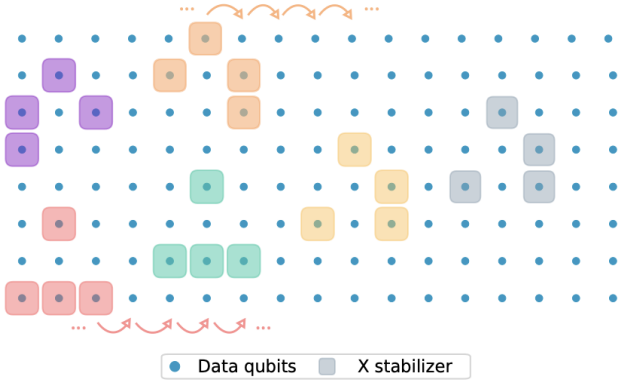
2. High threshold

3. LDPC codes can be local









Fowler et al. PRA 86 (2012)
D. Ruiz et al. arXiv:2401.09541 (2024)