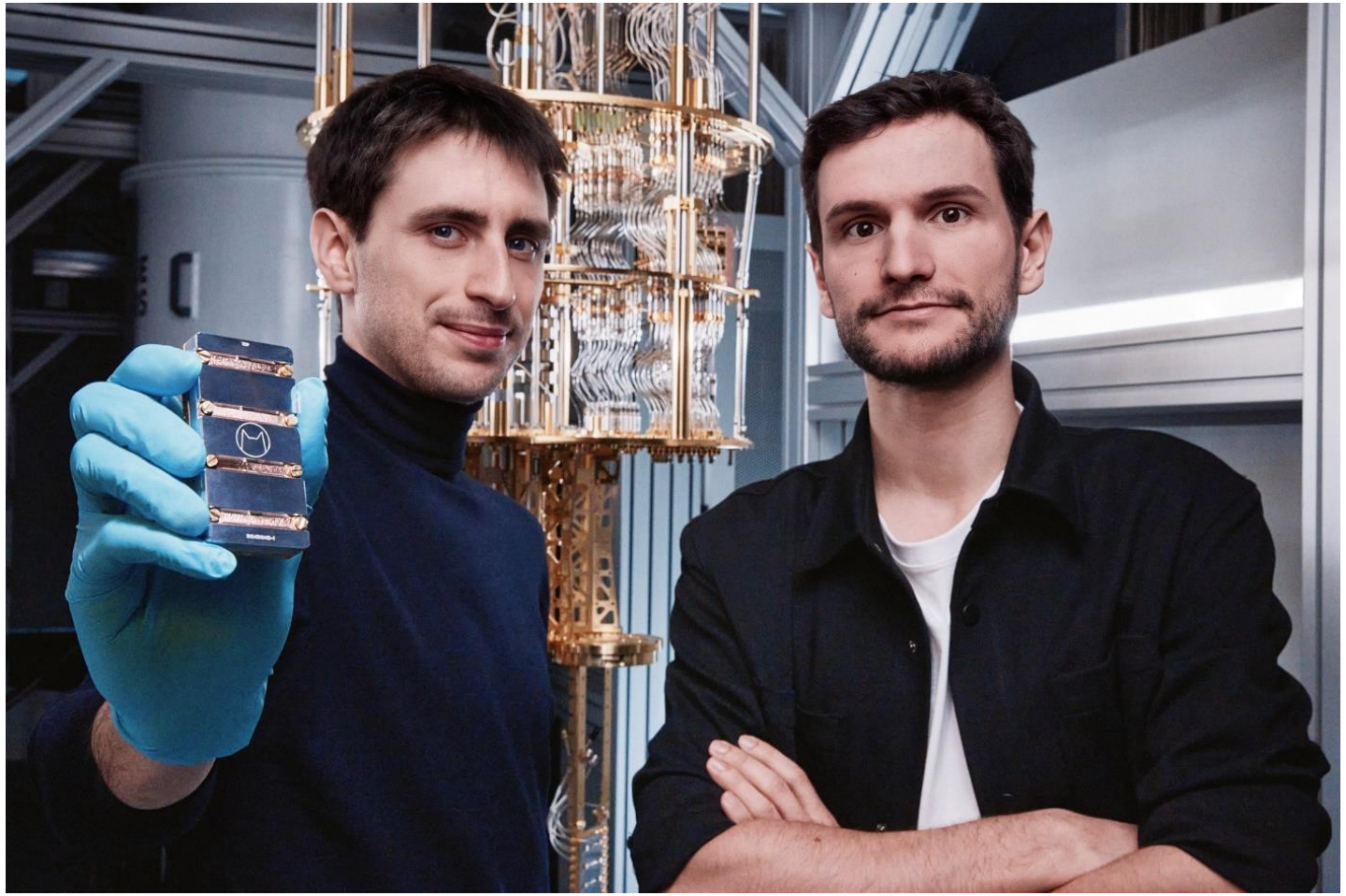
ALICE & BOB

SCALING CAT QUBITS WITH ENABLING TECHNOLOGIES

Rémi de La Vieuville

TQCI / September 5, 2024



Quantum computing revolution will be unlocked by error rate reduction.

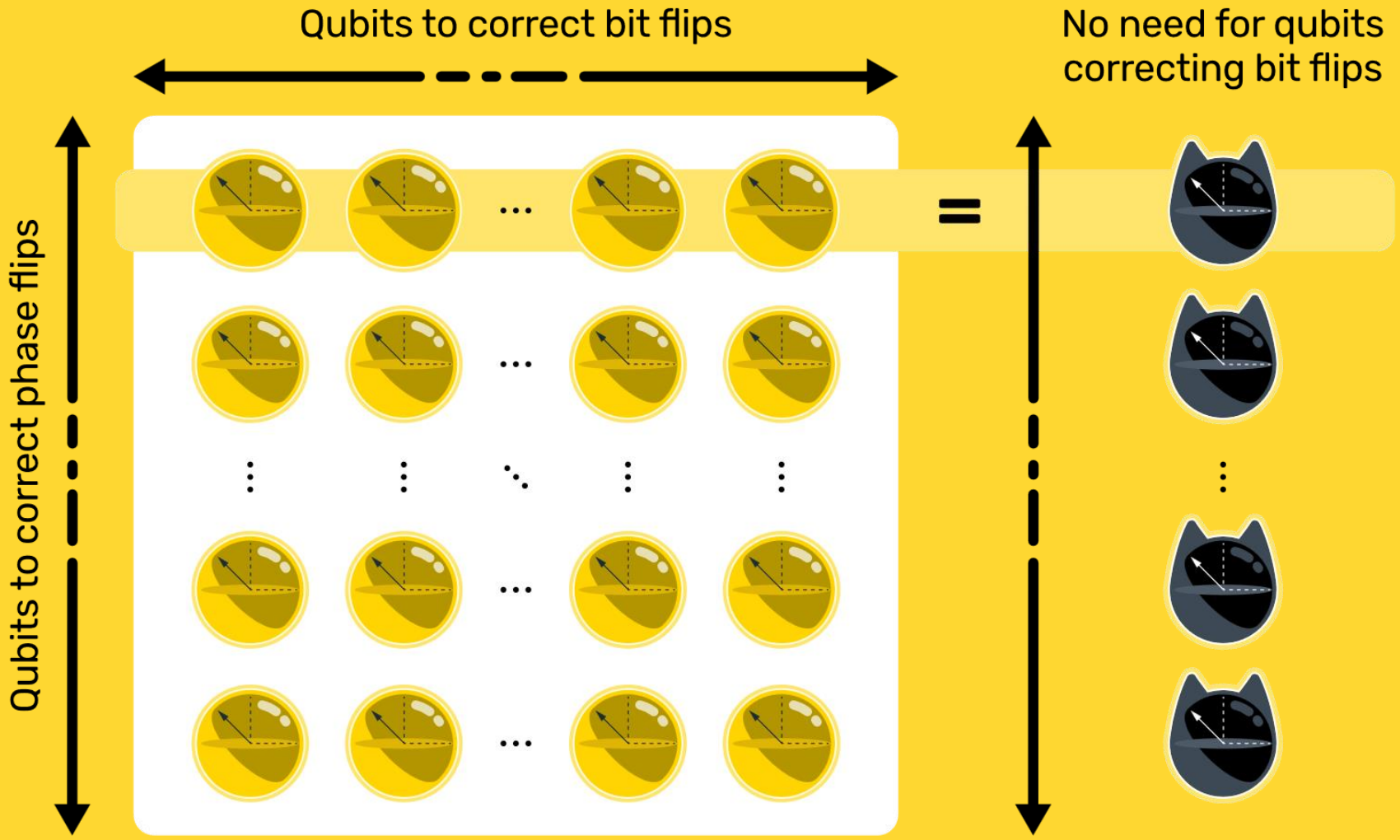
Enabling technologies is one of the main challenge for scalability.

.01

Scaling cat qubits

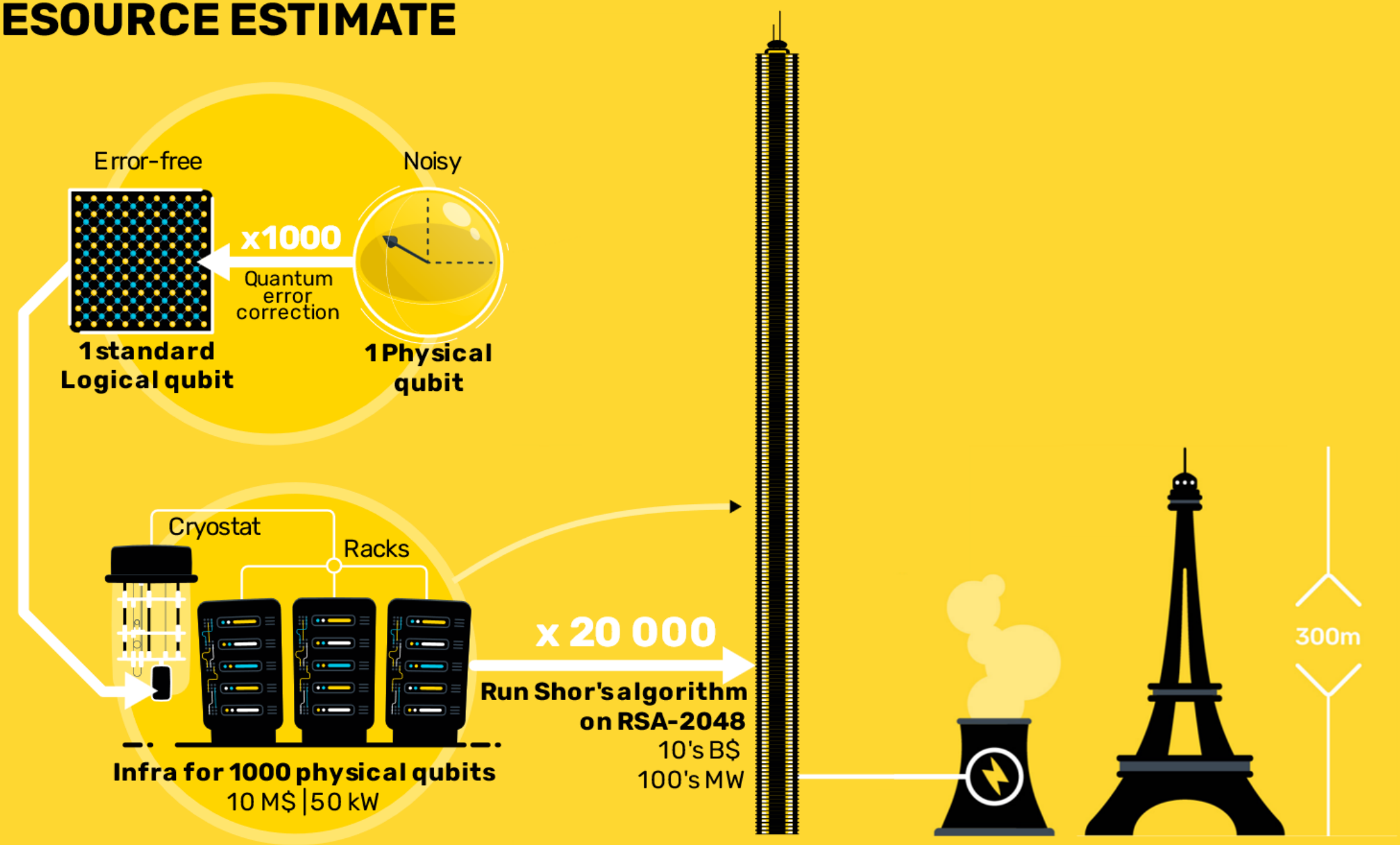
Cat qubits are hardware efficient

Subtitle of your slide



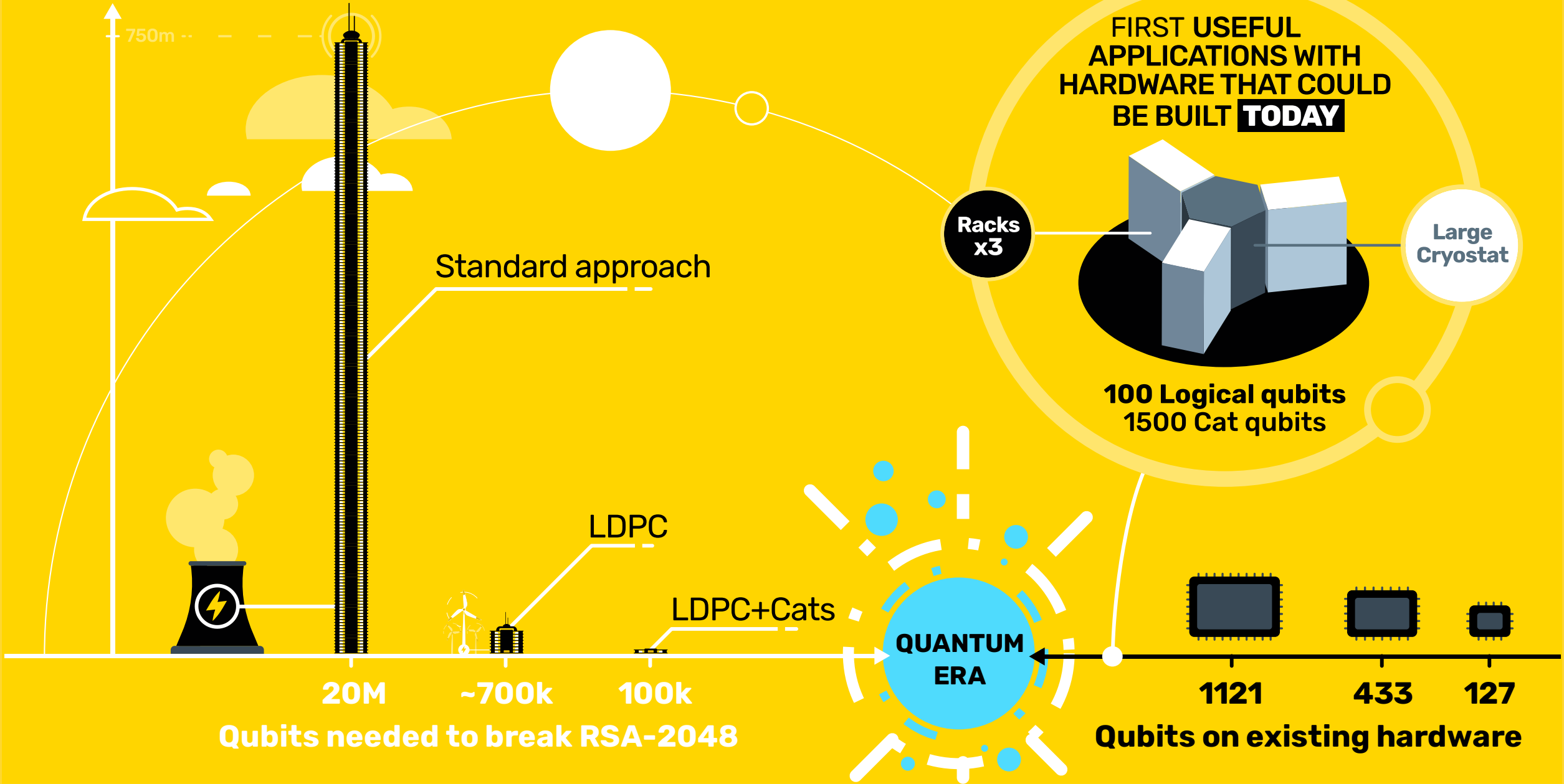
FULL-FLEDGED QUANTUM COMPUTER

RESOURCE ESTIMATE



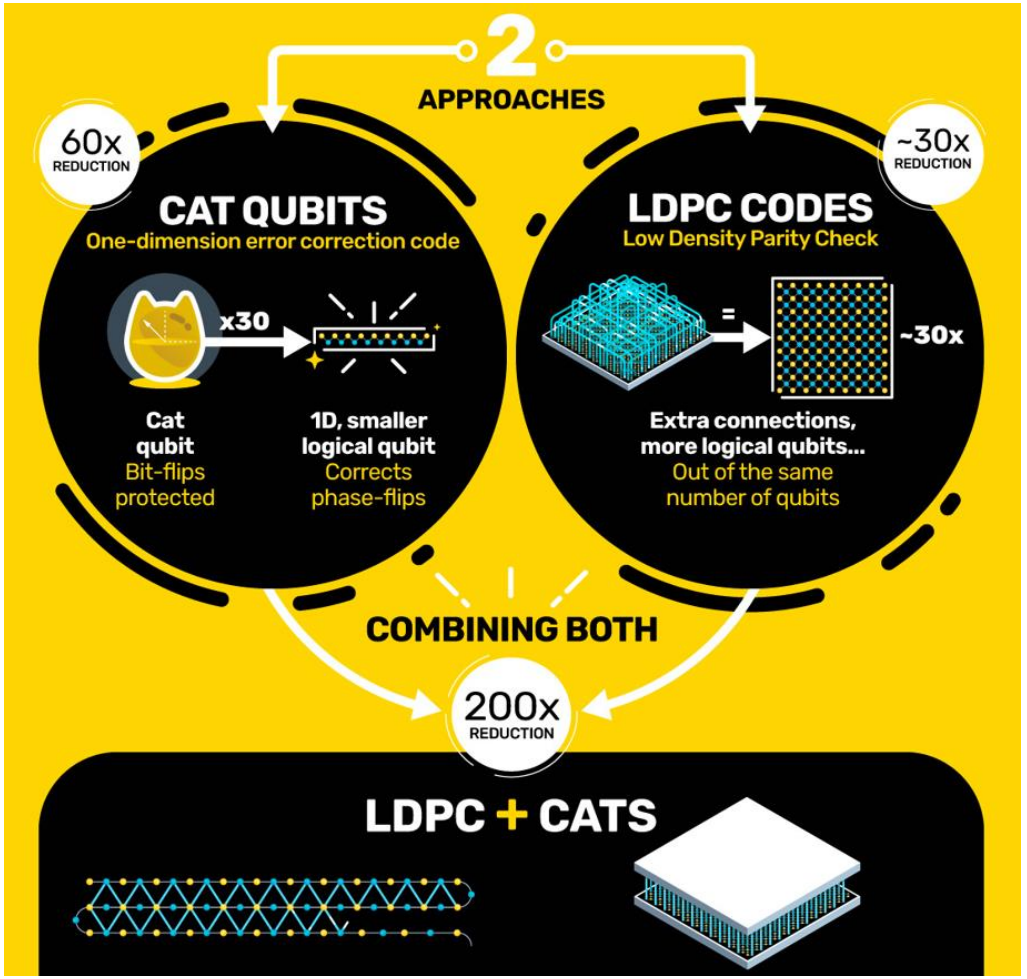
THE LAST DASH TO USEFUL QUANTUM COMPUTING

SAVING ON HARDWARE



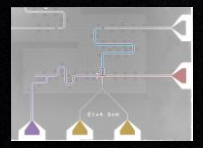
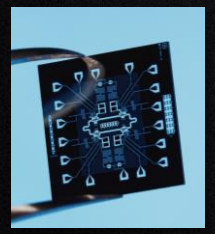
Alice & Bob latest research shows how to reduce the footprint of a powerful quantum computer by **200-fold**

It is one step further making quantum computing realistic, earlier



*In collaboration with **INRIA***

In 2026, our 40-cat chip will demonstrate FTQC

	1 Cat Qubit chip	4 Cat Qubit chip	Helium 1 16 Cat Qubit chip	FTQC demonstration 40 Cat Qubit chip
				
Tape out date	✓	END OF 2022	END 2023	MID 2025
Calibrating date	✓	END OF 2023	H2 2024	END OF 2026

Dev. phase: Escaping decoherence (Series A use of proceeds) → From logical qubit to logical processor (Series B use of proceeds)

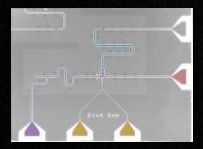
Key success factors

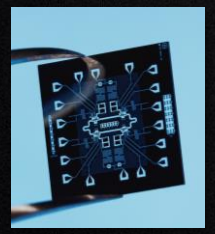
- ✓ Long lived logical qubit
- ✓ Entangling logical gates
- ✓ All-to-all logical connectivity
- ✓ Real-time error correction decoder
- ✓ Complete firmware platform

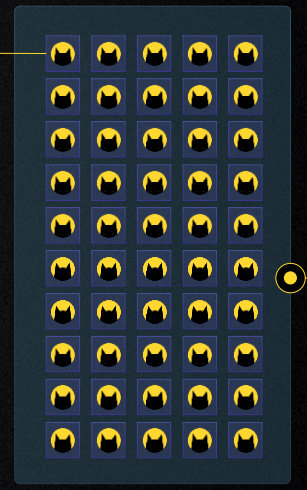
Ready-to-scale FTQC architecture

This demonstration will enable manufacturing outsourcing and architecture scaling to build the 1st FTQC

	1 Cat Qubit chip	4 Cat Qubit chip	Helium 1 16 Cat Qubit chip	FTQC demonstration 40 Cat Qubit chip	FTQC	Large scale FTQC
					Key challenge: Improve chip manufacturing yield	Key challenge: Miniaturize classical control electronics
					100 logical qubits over 1,500 cat qubits	40-cat qubit chip[1] **x400**
Tape out date	✓	END OF 2022	END 2023	MID 2025	2028	2030
Calibrating date	✓	END OF 2023	H2 2024	END OF 2026		



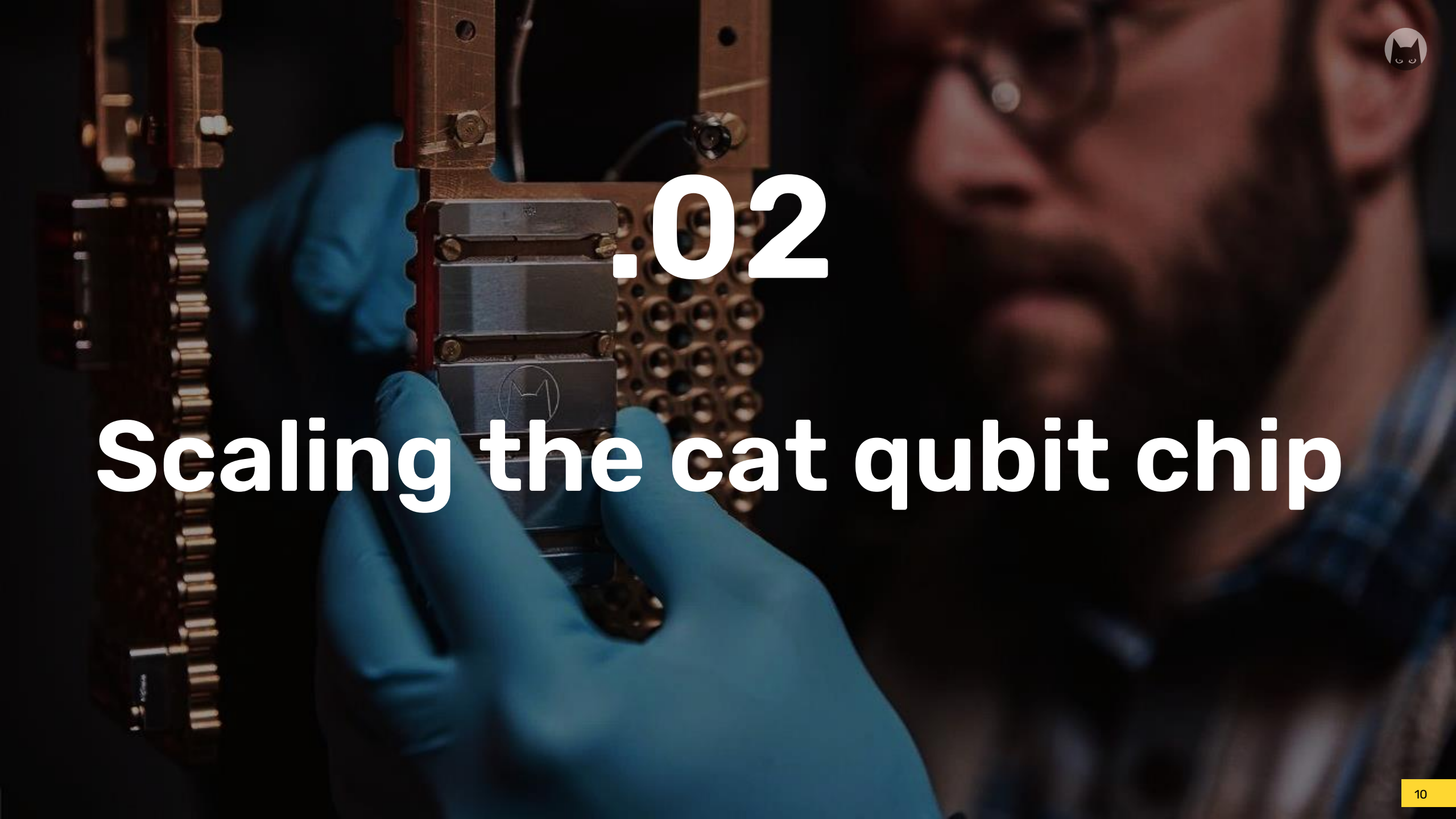




Dev. phase

- Escaping decoherence (Series A use of proceeds)
- From logical qubit to logical processor (Series B use of proceeds)
- Towards full-fledge quantum computer

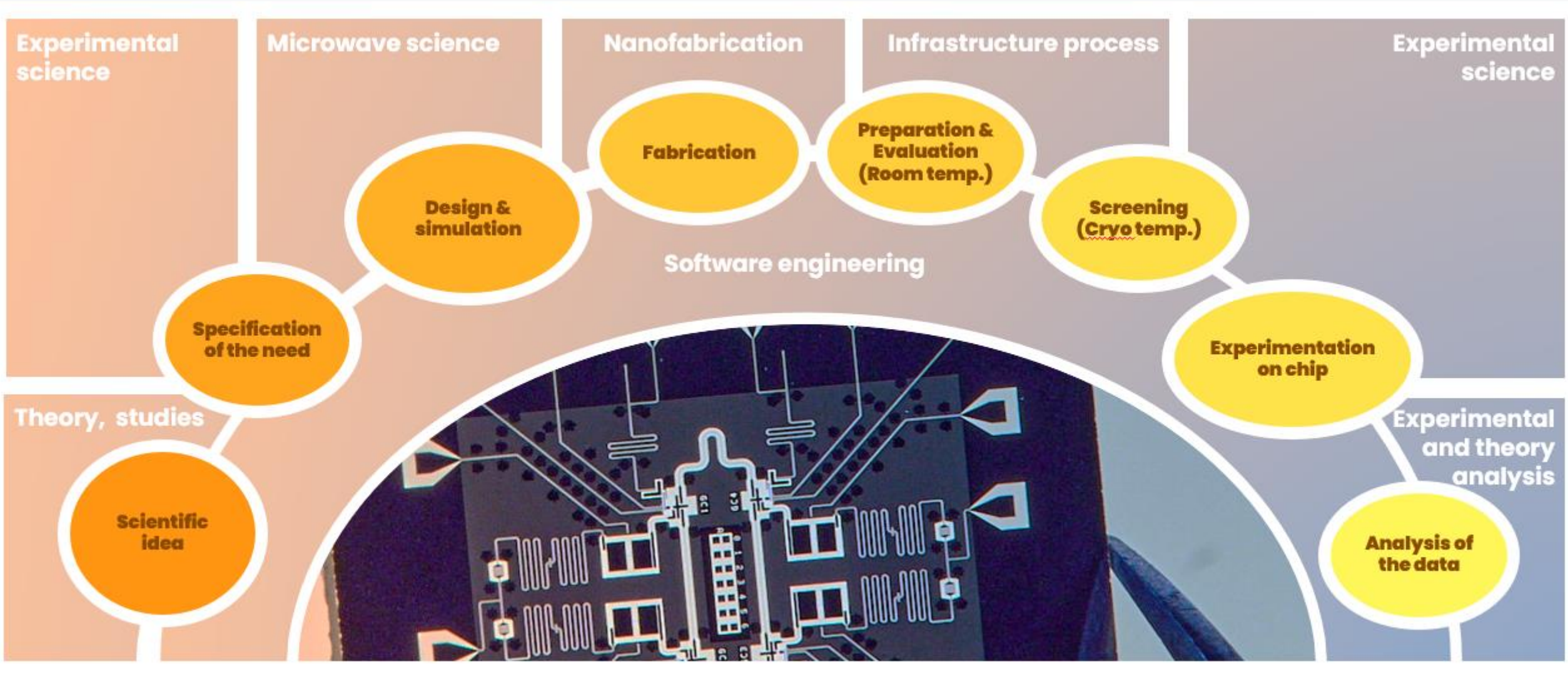
Note
1. Architecture improvement will likely significantly reduce the number of required cats



.02

Scaling the cat qubit chip

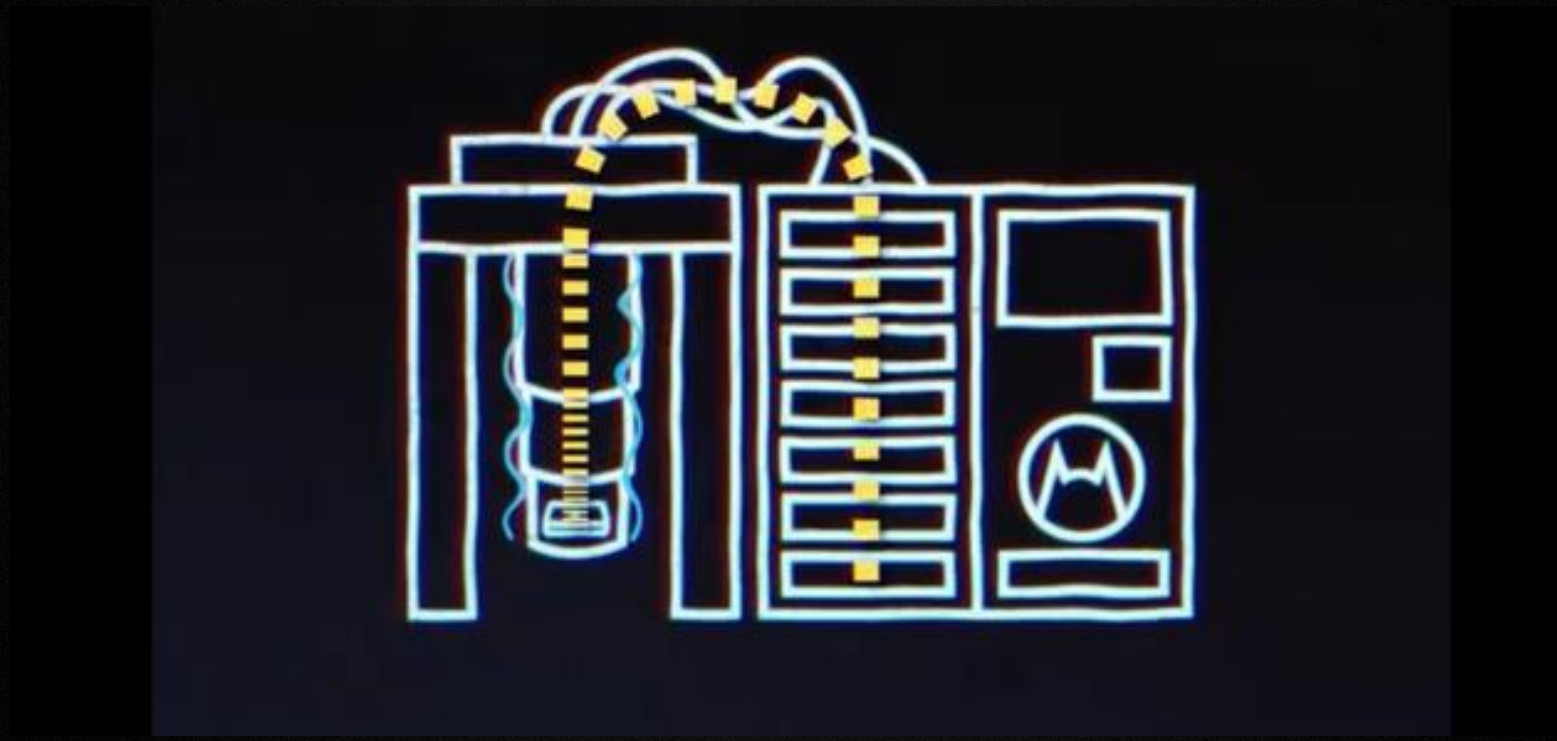
Sca


Experimental science
Microwave science
Nanofabrication
Infrastructure process
Experimental science
Fabrication
Preparation & Evaluation (Room temp.)
Design & simulation
Screening (Cryo temp.)
Software engineering
Specification of the need
Experimentation on chip
Theory, studies
Experimental and theory analysis
Scientific idea
Analysis of the data

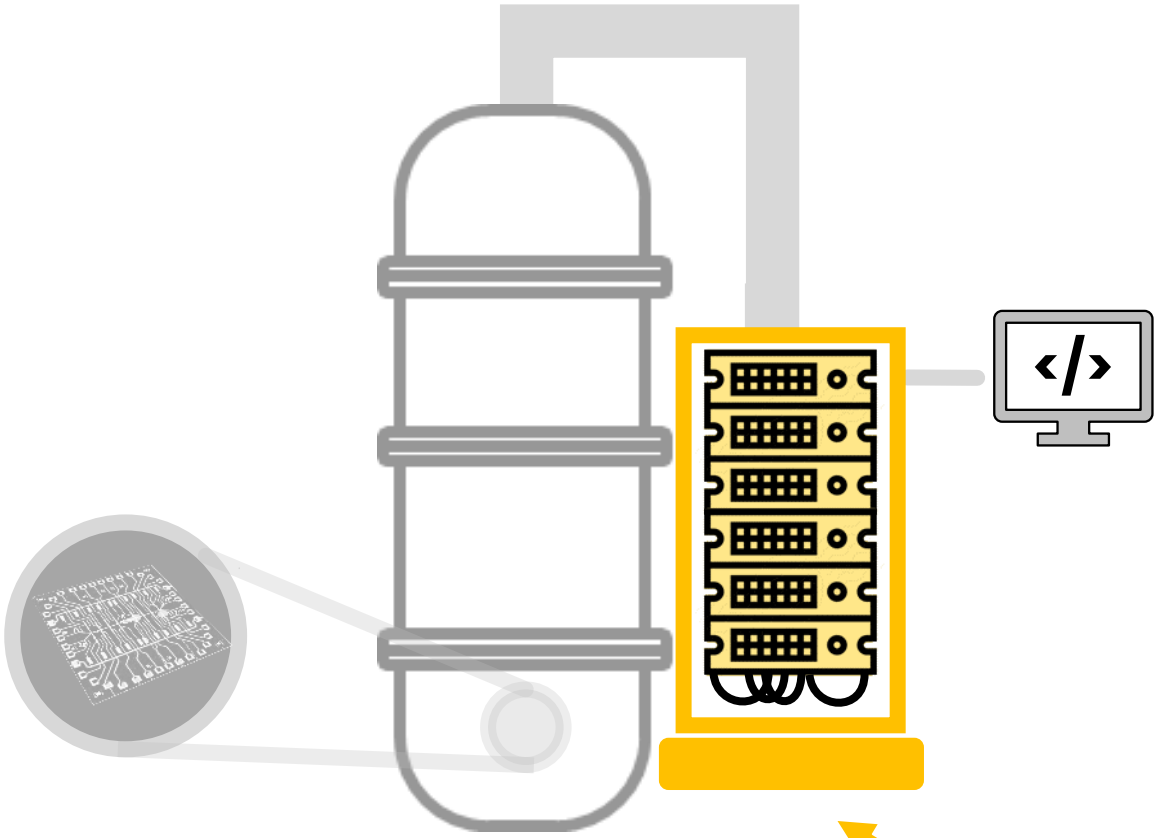
.03

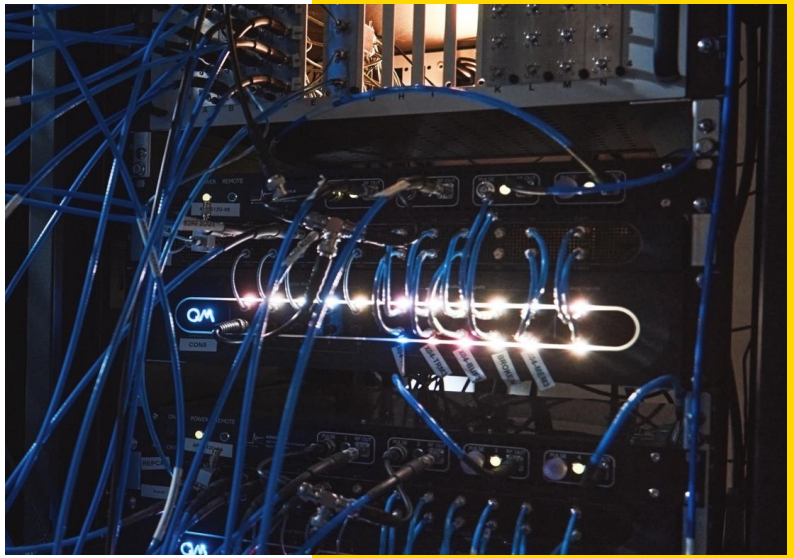
Scaling enabling technologies

The example of Control Electronics



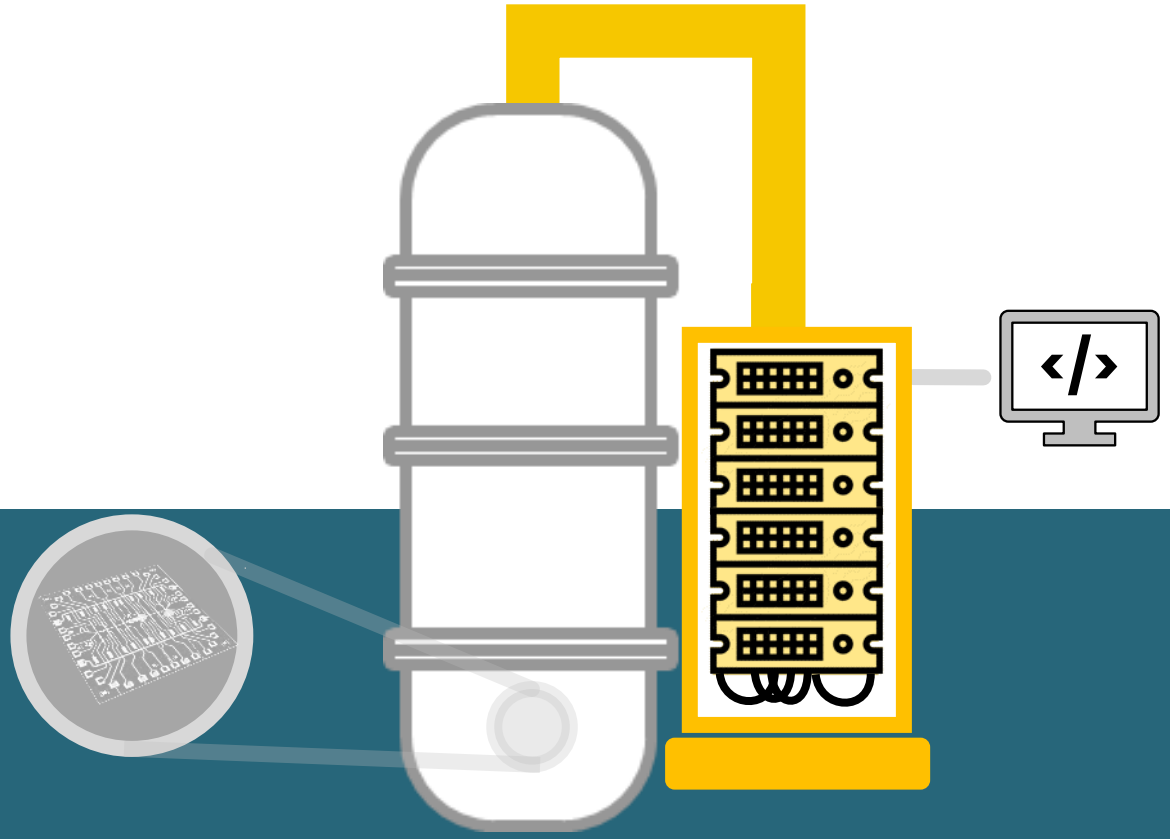
Control Electronics

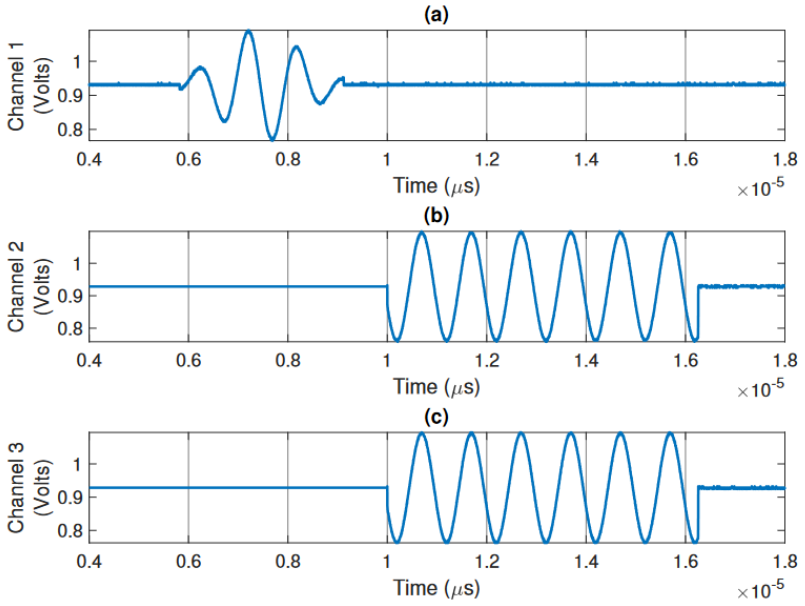




OPX+ , Octave, APMS

Cat qubits need pulses





To stabilize and operate cat qubits, pulses are sent through RF channels (carrier @4-9GHz).

There is an extreme need of phase coherence between output channels.

Similarly, input channels receive pulses to enable feedback on next pulses to be sent.

DDS architecture

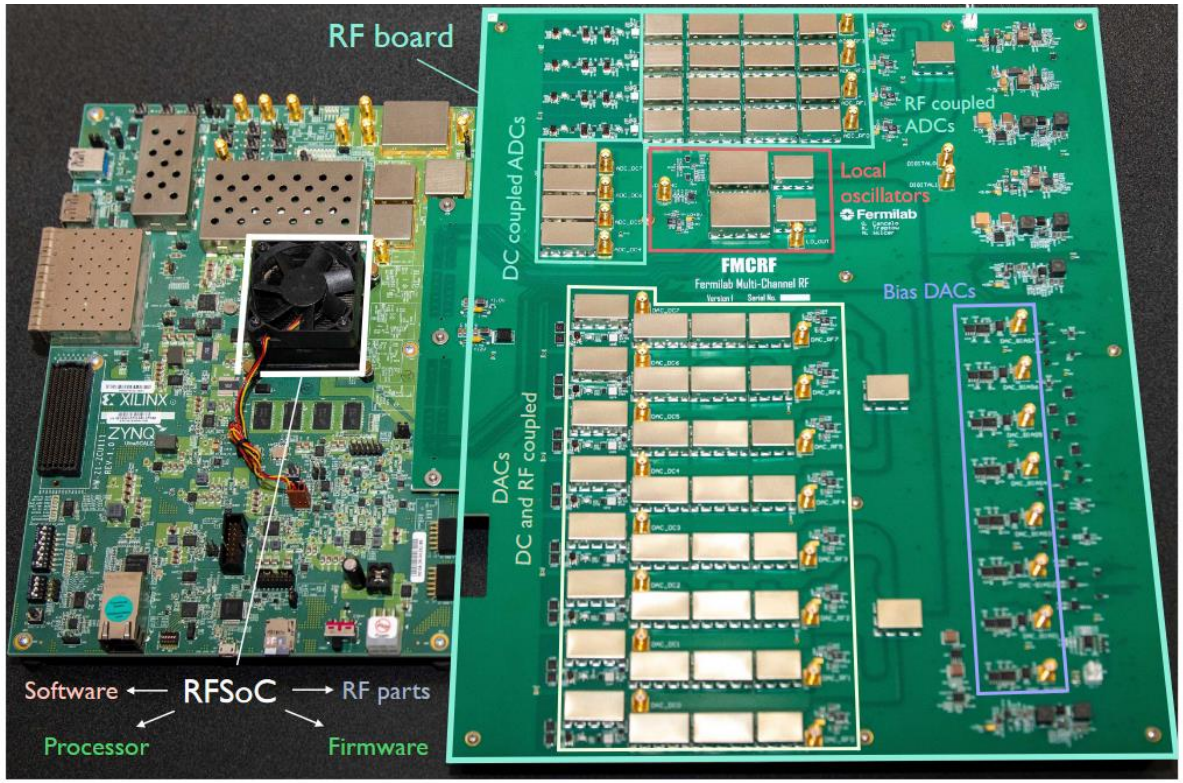
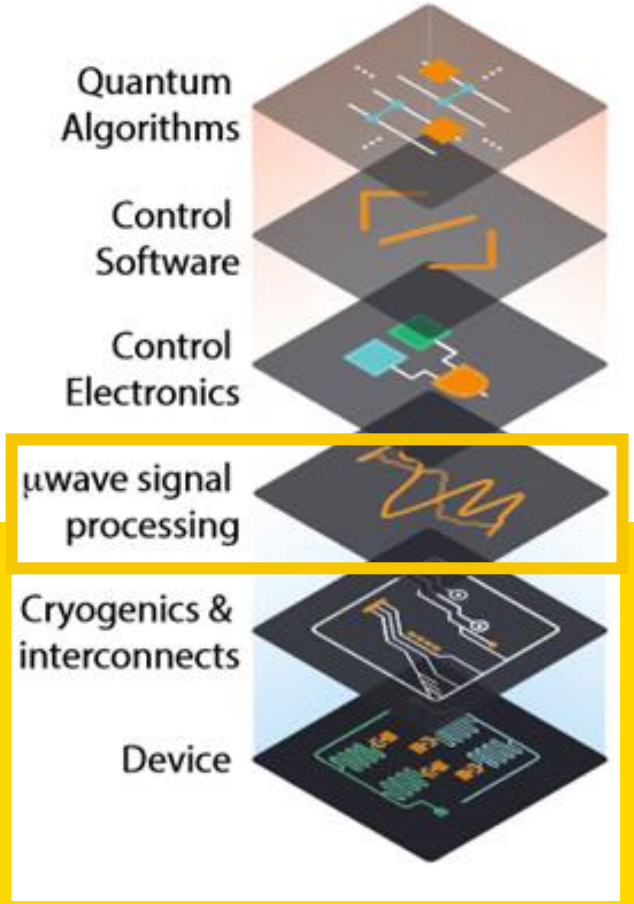


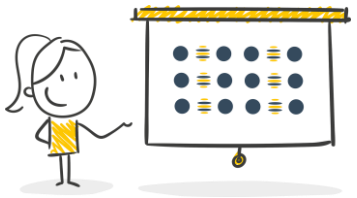
FIG. 1. The Quantum Instrumentation Control Kit (QICK). The QICK consists of two pieces of hardware: the commercial ZCU111 RFSoC evaluation board (left), which connects to the QICK RF board (right) which can be used for additional signal up/downconversion, amplification and filtering.

Direct Digital Synthesis use RF DACs that operates at high enough sampling rates that enable to directly synthesize microwave pulses without upconversion.

Example : QICK [2022]

Analog quality

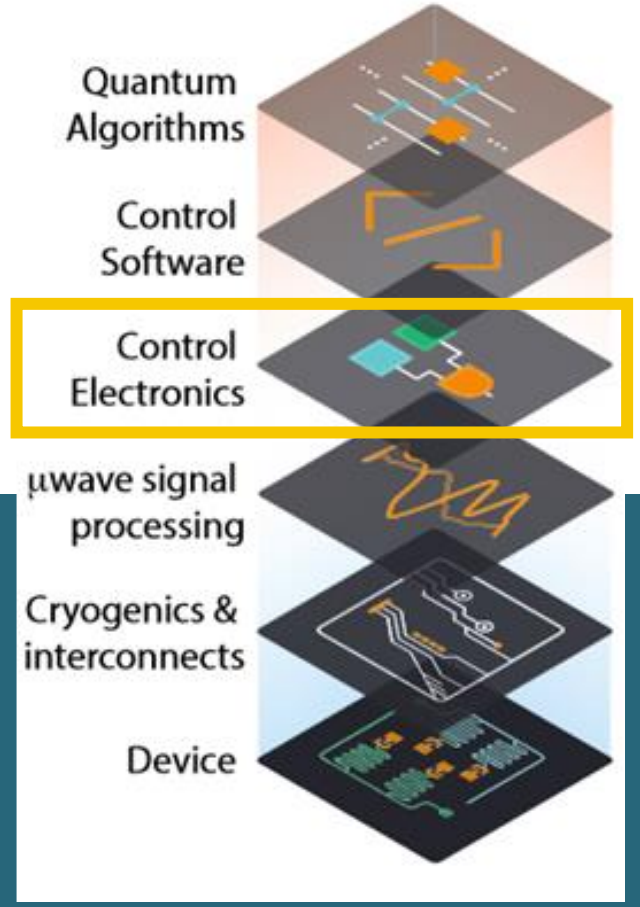


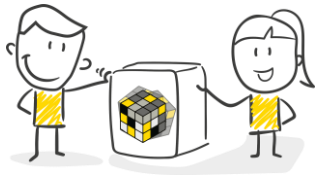


Analog quality is measured through :
- Frequency precision and stability
- Bandwith
- Spectral purity
- Phase noise
- Amplitude deviation
- Jitter
- Possible artifacts
- Power efficiency

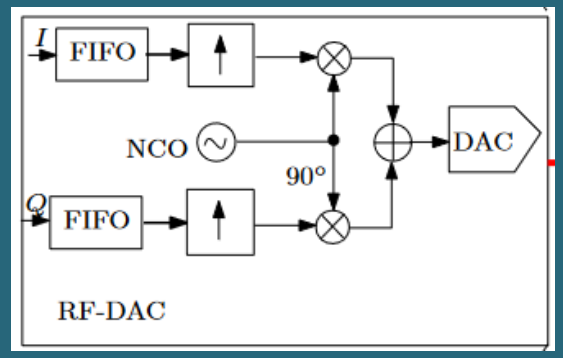
Those needs and bandwith range
are very similar to **5G / radars requirements**.

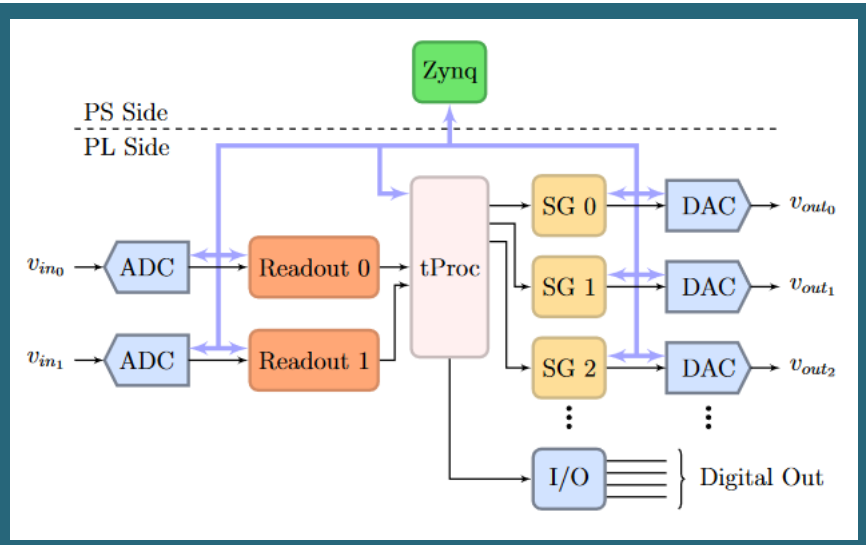
Digital expressiveness





FPGA main buiding blocks are typically **:**
- NCO
- Digital up/downconversion
- Pulse library
- Processor for custom timed instructions
- Feedback logic
- I/O





Control electronics will soon face obstacles to improve phase coherence, latency, density, and **scalability**

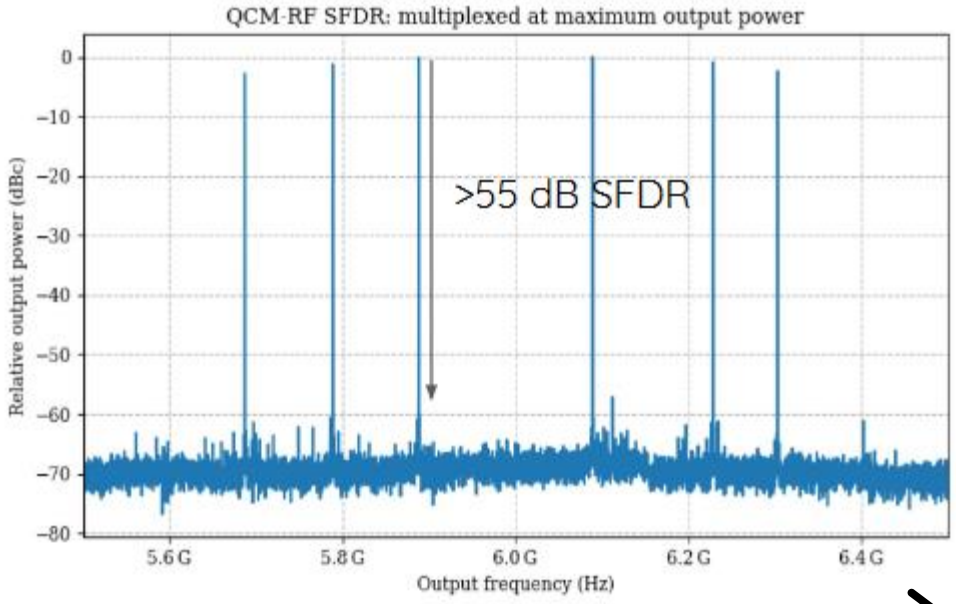
Core competences rely on generating high quality **RF pulses**

#1 Defining analog quality

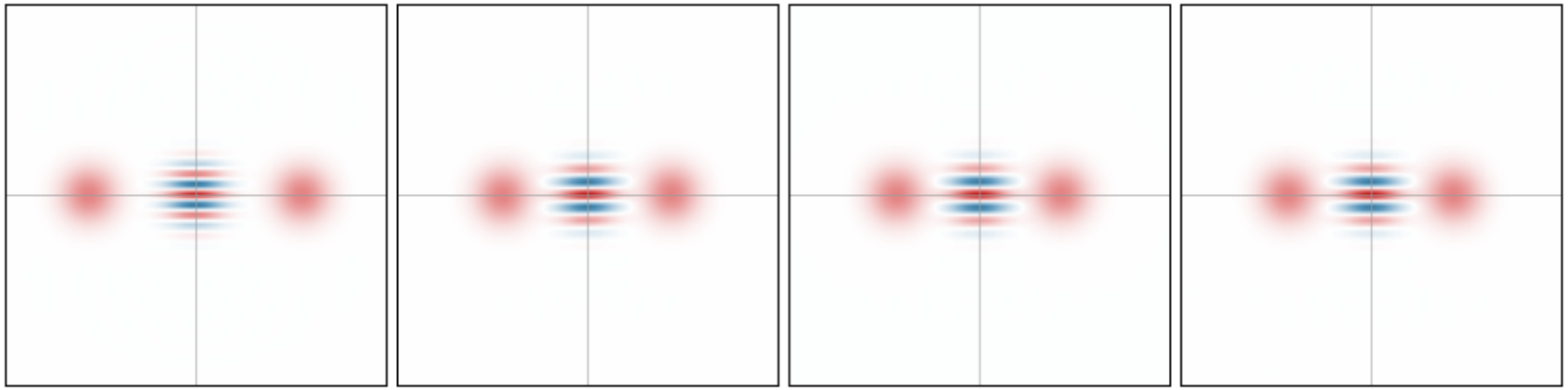
$$s_1(t) = A_1 cos(\underbrace{\omega_1 t + \phi_1^{init}}_{phase})$$

$$s_1(t) = A_1 cos(\underbrace{\omega_1 t + \phi_1^{init}}_{phase})$$

$$s_1(t) = (A + \delta A_{cst} + \delta A(t) + \delta A_{rel}(t)) \, cos((\omega + \delta\omega_{cst} + \delta\omega(t) + \delta\omega_{rel}(t)) \, t + (\phi + \delta\phi_{cst} + \delta\phi(t) + \delta\phi_{rel}(t)))$$



From control electronics quality metrics to cat qubit fidelity



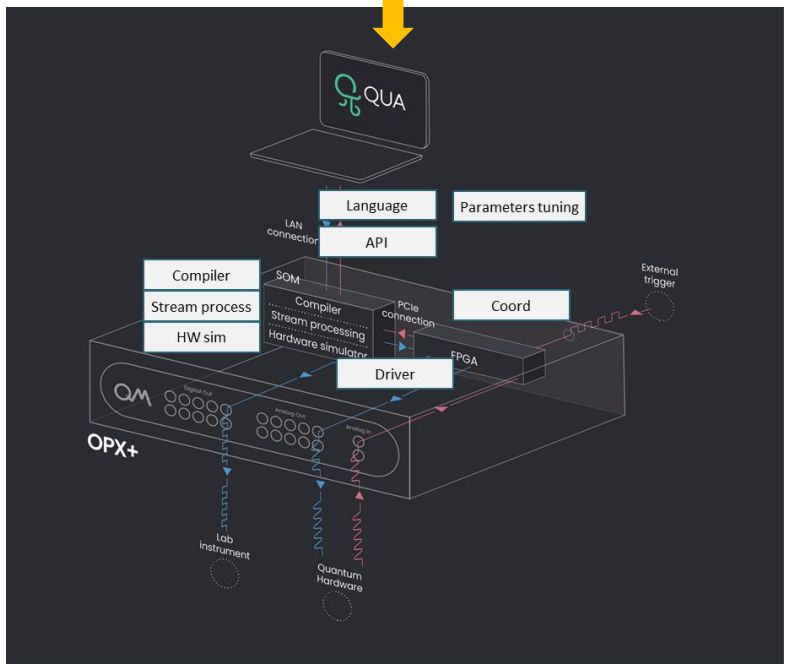
dynamiqs

#2 Challenges with SW integration

Measures

EXP TOOLS

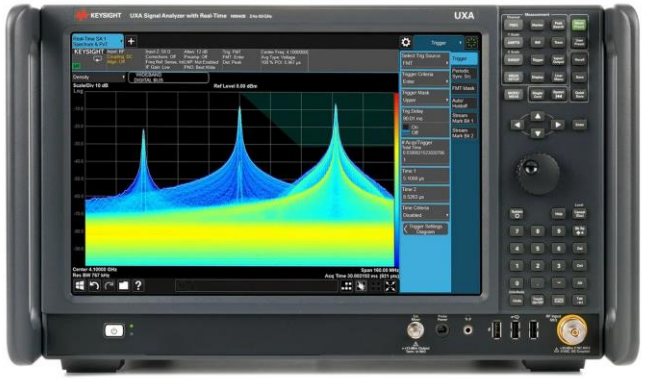
Integration layer



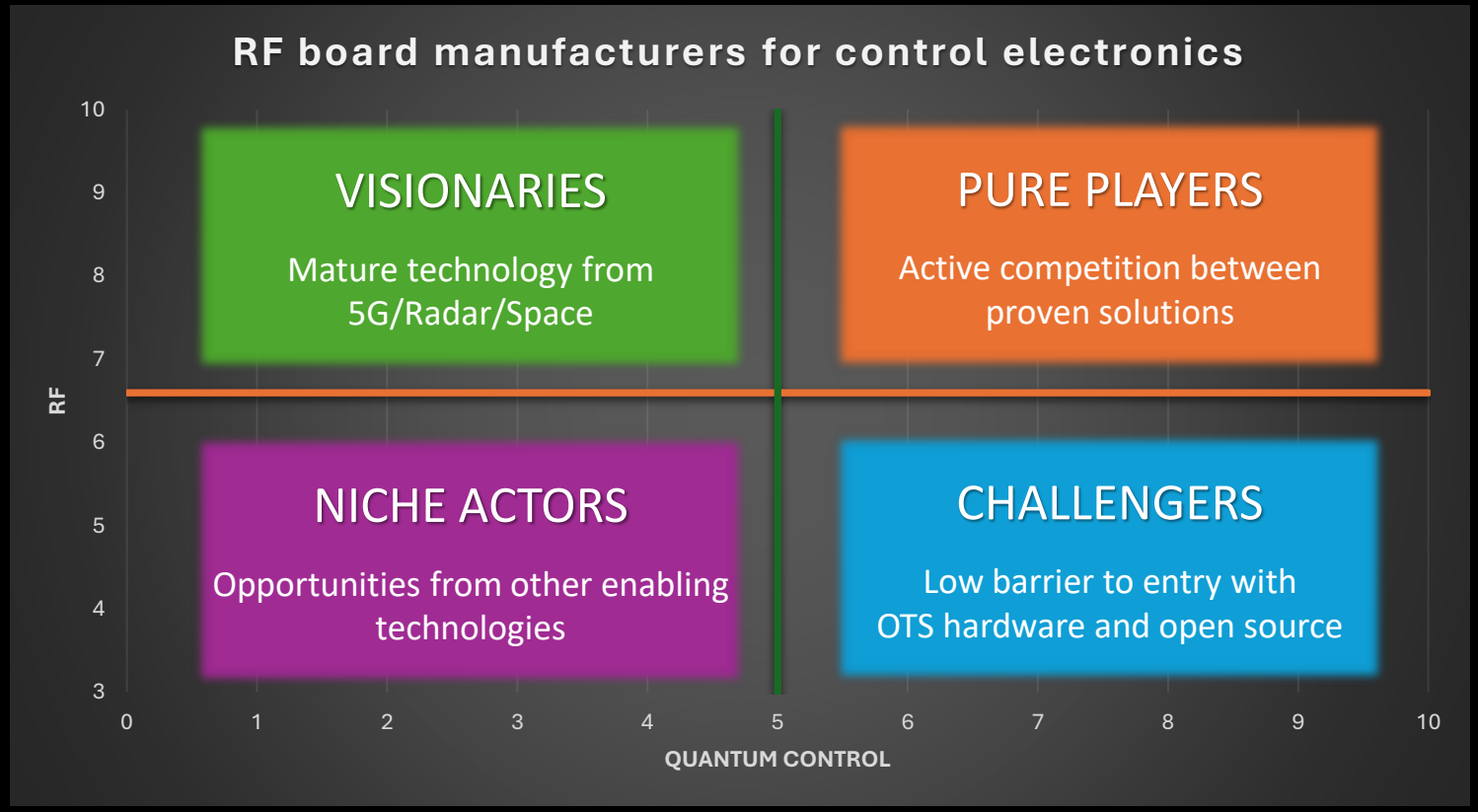
#3 Defining testbench needs

QuantrolOx

PQSC


KEYSIGHT
UXA Signal Analyzer with Real-Time
UXA

#4 Assessing the ecosystem



[Orange Leaders]

[Blue challengers]

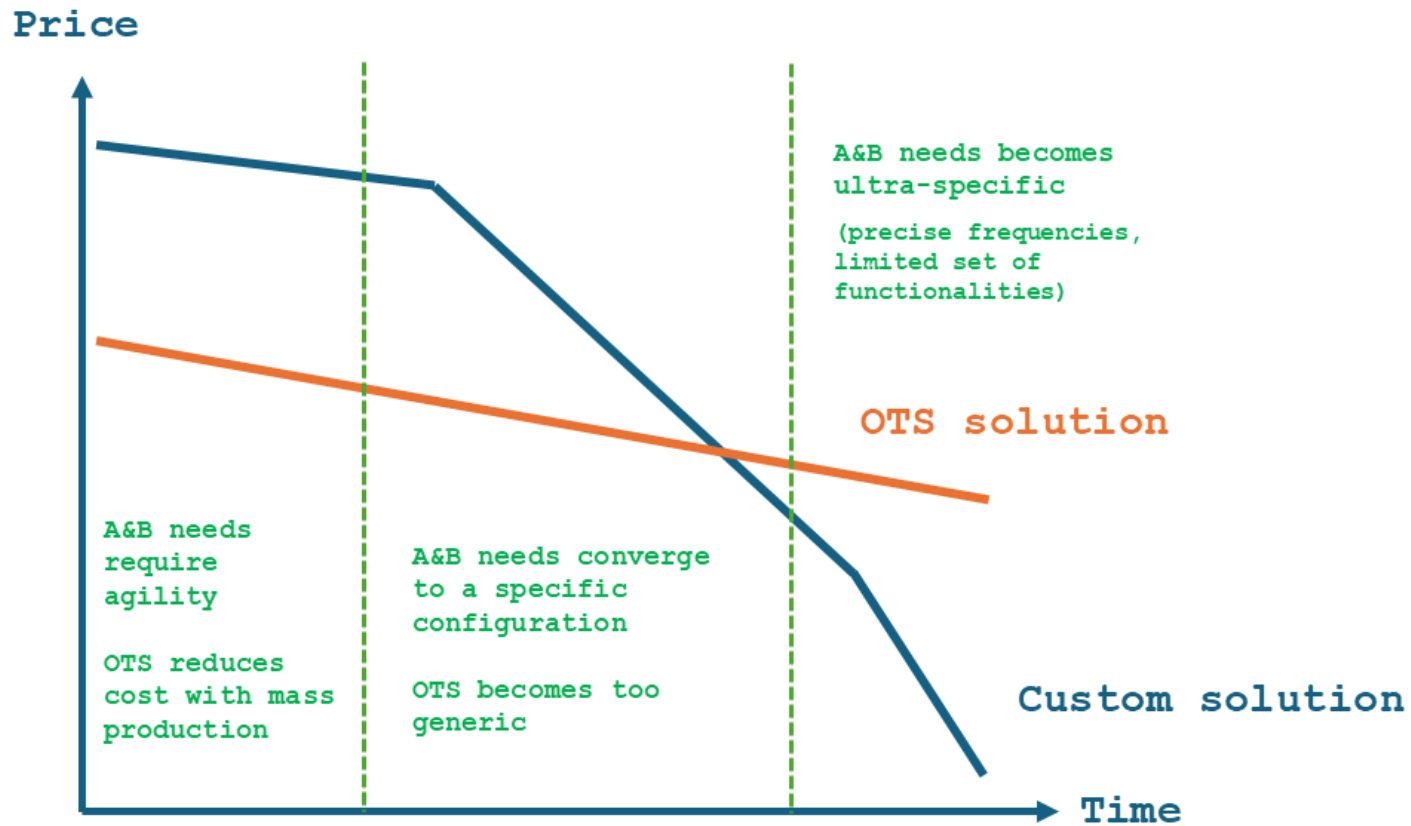
[Green visionaries]

[A&B specs]

[Tech giants]

[New paradigms]

#5 Defining a strategy (« Make or buy »)



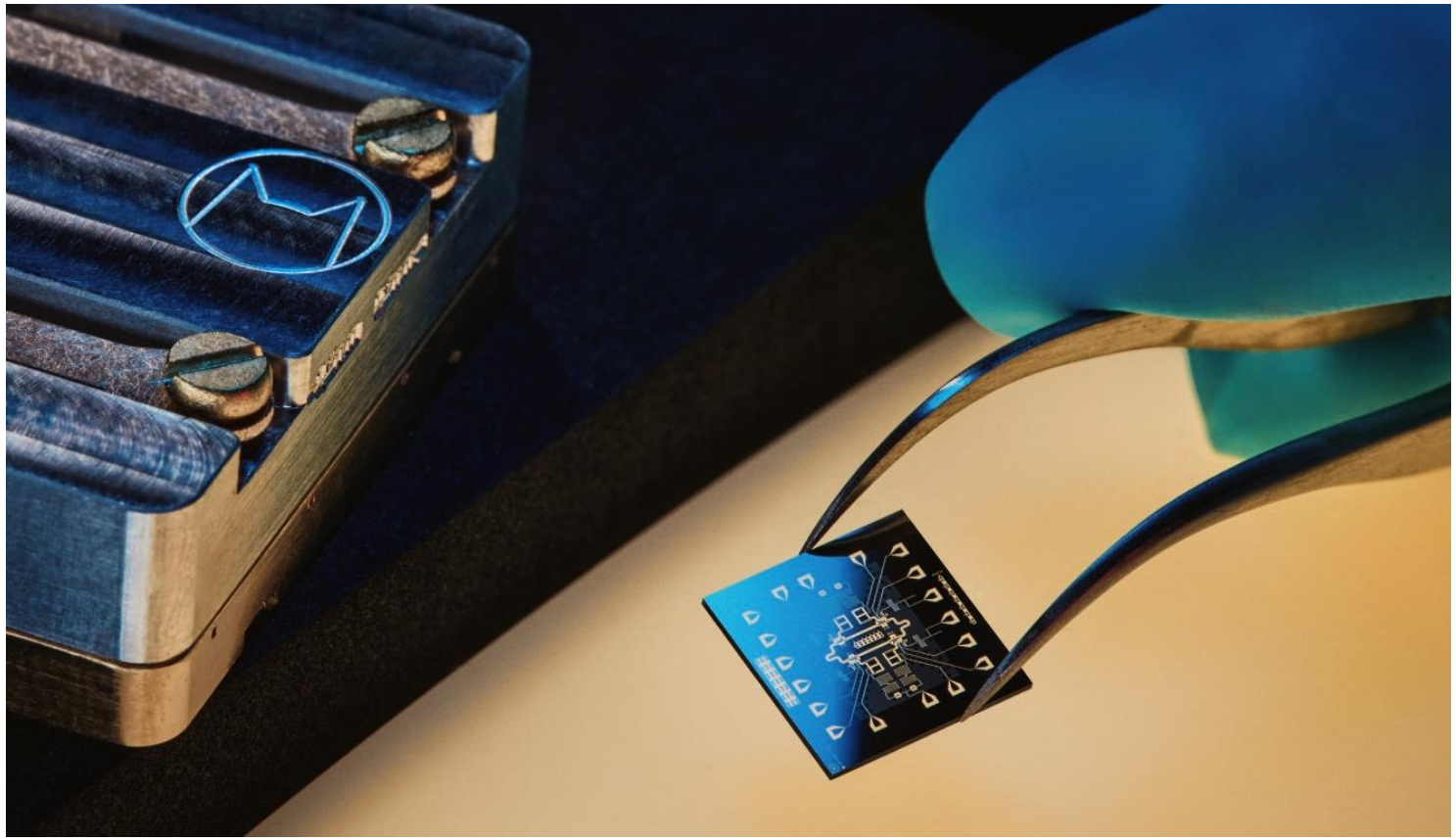
CONFIDENTIAL

Partnerships

Partnerships will enable to explore **new paradigms** to control cat qubits at scale

- RF signal processing
- ASIC
- Error Correction

- CryoCMOS
- Optics
- SFQ
- Superconducting



THINK
INSIDE
THE BOX