

Post-K Supercomputer with Fujitsu's Original CPU, Powered by ARM ISA

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Outline

FUjitsu

Fujitsu's HPC solutions
 Post-K development

 Goals and approach of Post-K
 Software and applications

 Summary

Fujitsu Supercomputers ARM Fujitsu has been providing high allelies FX100 Nassively Para Nassively Para upercomputer performance supercomputers for 40 years, increasing application performance while **FX10** Post-K maintaining application compatibility Under Development No.1 in Top500 (June and Nov., 201 Vector Supercomputer World's Fastest **Most Efficient** Vector Processor (1999) Performance **VPP5000** SPARC in Top500 (Nov. 2008) NWT* Enterprise **Developed** with NAL PRIMEQUEST No.1 in Top500 **VPP300/700** (Nov. 1993) PRIMEPOWER PRIMERGY CX400 **Gordon Bell Prize** Skinless server HPC2500 (1994, 95, 96)**VPP500** World's Most Scalable PRIMERGY **VP** Series **BX900** Supercomputer **Cluster node** (2003)AP3000 HX600 F230-75APU **Cluster node PRIMERGY RX200** AP1000 **Cluster node** Japan's Largest Japan's First **Cluster in Top500** Vector (Arrav) (July 2004) Supercomputer *NWT: Numerical Wind Tunnel (1977) 19901995 2000 2005 2010 2015 ~1985

Fujitsu HPC Solutions to Meet Customer Demands Fujits

- Providing supercomputers w/ Fujitsu-developed CPU & x86 clusters
 High performance, high scalability, and high reliability
- "Single system image" operation w/ Fujitsu system software
 - Post-K is being developed to focus on high application performance and low power consumption
 - State-of-art technologies & additional features for the future



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Achievements with the K computer

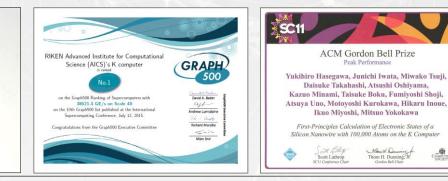


- Prestigious Benchmark Awards
 - TOP500: 10.5Pflops, 93% efficiency
 - HPCG: 602Tflops, 5.3% efficiency No. 1
 - Graph500: 38.6TTEPS

at SC16 6 years from the initial delivery

- HPC Challenge Class 1: No.1 in all categories No. 1 (1) Global HPL, (2) Global Random Access, (3) EP STREAM, (4) Global FFT
- Gordon Bell Prize Awards
 - "First-Principles Calculation of Electron States of a Silicon Nanowire with 100,000 Atoms on the K computer" (2011)
 - "4.45 Pflops Astrophysical N-Body Simulation on K Computer The Gravitational Trillion-Body Problem" (2012)
 - "Simulations of Below-Ground Dynamics of Fungi: 1.184 Pflops Attained by Automated Generation and Autotuning of Temporal Blocking Codes" (2016 finalist)





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Latest News from ISC17 Last Week

K computer kept #1 positions for Graph500 & HPCG





Post-K would be a very worthy successor to the K computer heritage

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Post-K Goals and Approaches



Post-K Goals

- Attains high application performance and good power efficiency
- Keeps application compatibility while advancing from predecessors
- Provides good usability and better accessibility for users

Our Approaches

- Develops high performance and scalable CPU w/ custom designed CPU core
- Maintains performance balance for application compatibility & performance
- Adopts ARM ISA and its standard frameworks

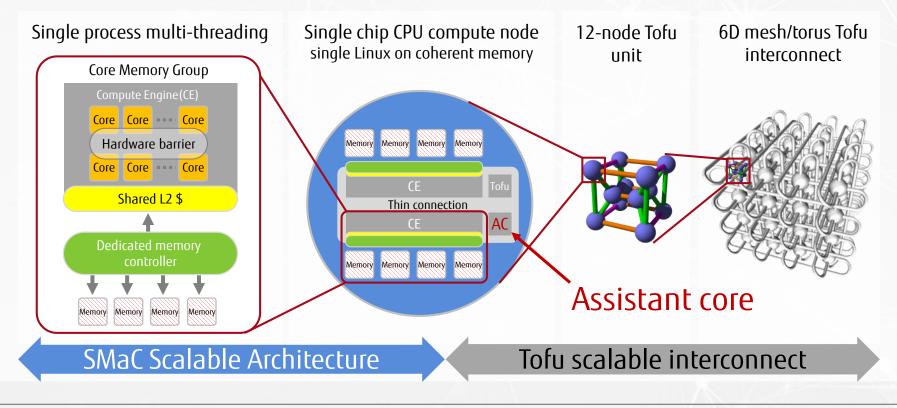
High & Scalable Performance Introduced in FX100 Fujirsu

A scalable, many-core micro architecture concept, "SMaC"

Assistant core for OS daemon and MPI offload to minimize OS Jitter

Tofu interconnect enables the larger configuration w/ scalability

Conceptual architecture of FX100 and beyond

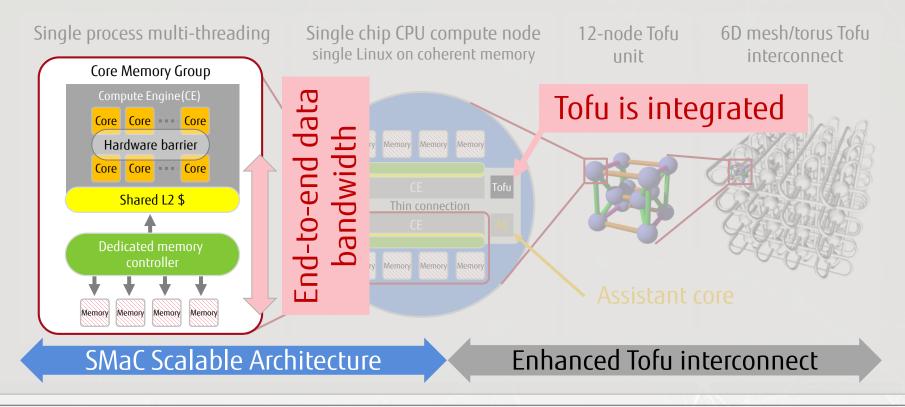


Performance Balance Realized in FX100



End-to-end data bandwidth by SMaC
 Tofu interconnect is integrated into the CPU

Conceptual architecture of FX100 and beyond



Adopting ARM Standard Architecture



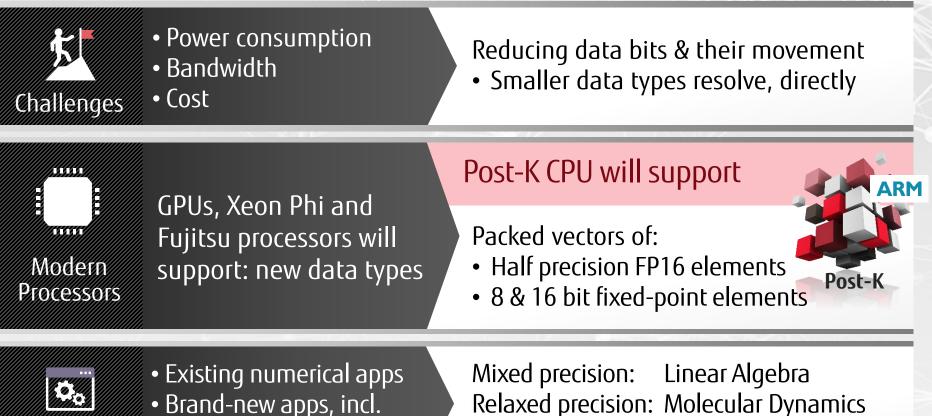
ARMv8-A with SVE

- The latest HPC extension promises the high performance codes
- Co-operate with ARM communities and utilize OSS
 - Linaro, OpenHPC, OpenSFS, Open MPI, OpenMP, and etc.
 - Contribute our experiences w/ HPC applications and optimization
- Getting involved in the ARM HPC ecosystem by providing high performance machines in applications and low power consumption
- ARM's standard frameworks, SBSA, SBBR, etc.
 - Assure software compatibility among ARM platforms

Post-K Supports a New Data Type: FP16



FP16 is one of the key features for further optimization opportunities regarding hardware, system software, and applications



deep learning

Applications

Molecular Dynamics Relaxed precision: Half precision: **Deep Learning**

Post-K Hardware Features

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Fujitsu CPU cores support the ARM SVE instruction set architecture

- Fujitsu CPU & Tofu maintain the programming models and provide high application performance
- FP16 ("giant vector throughput") for supercomputers

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	Functions & architecture	Post-K	FX100	FX10	K
CPU Core	Instruction set architecture	ARMv8-A	SPARC V9		
	SIMD width	512bit	256bit	128bit	128bit
	Double precision (64bit)	 Image: A start of the start of	~	~	~
	Single precision (32bit)	 Image: A start of the start of	~	~	~
	Half precision (16bit)	 ✓ 	-	-	-
Interconnect	Tofu interconnect	Enhanced	Tofu2	Tofu	Tofu

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Post-K Software Stack

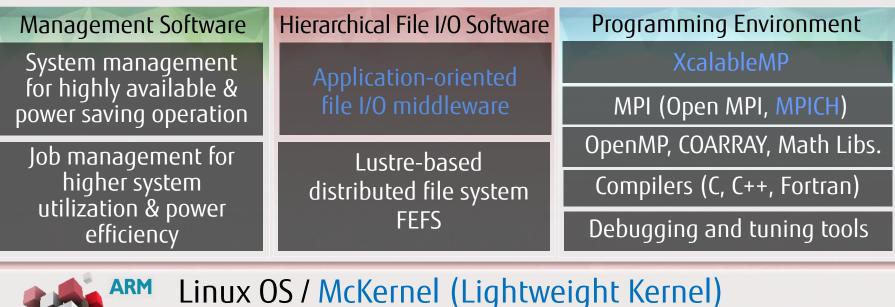
Under Development



Valuable feedbacks through "co-design" from application R&D teams

Post-K Applications (in next slides)

FUJITSU Technical Computing Suite / RIKEN Advanced System Software

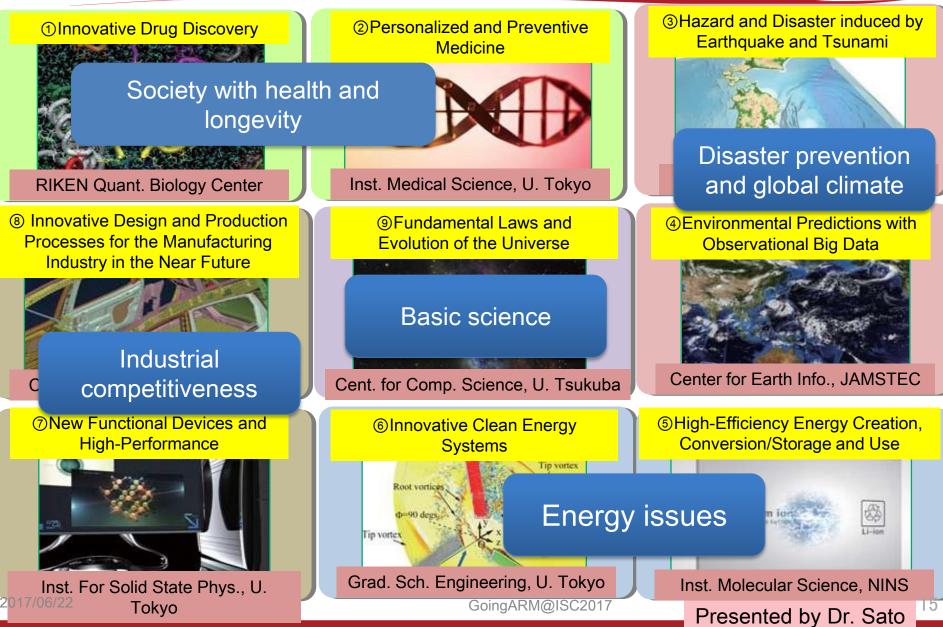


Post-K System Hardware



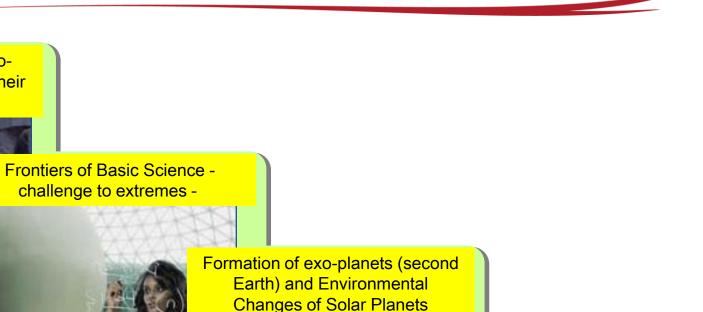
Target science: 9 Priority Issues







Interactive Models of Socio-**Economic Phenomena and their Applications**





Changes of Solar Planets



Mechanisms of Neural Circuits for Human Thoughts and Artificial Intelligence

AICS

RIKEN



GoingARM@ISC2017



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ARM Linaro



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