HPC Hackathon

Industrial code optimization

Principle

We aim with this hackathon to bring together Master II-level HPC students in a virtual competition around computational codes provided mostly by Electricité De France - EDF (Saturn and Telemac code) and CGG (seismic core).

This competition will rely on Amazon Web Services - AWS instances based on Arm technologies. Indeed, the target architectures (AWS Graviton 2 and 3 processors) offer certain approaches (software ecosystem, design) that motivate a specific effort compared to traditional Intel or AMD type architectures. Typically, on the Graviton 3 processor, we can mention the use of SIMD units (Scalable Vector Extension/SVE compared to AVX2 or AVX-512 on x86 architectures) or the availability of 8 DDR5 memory channels.

This hackathon is structured around computational codes, software environments and hardware solutions that have already been tested by industry. The compilation recipes and optimization phases have been validated before the event. The students will therefore be in a framework close to a guided practical session with the opportunity to increase their understanding of industrial issues around high-performance simulation. No specific contributions from students in terms of porting or optimization are expected (these codes are largely proven in a production context and on multiple hardware architectures). The participants will nevertheless be credited by the industrial partners (the codes have an open status) in case of significant advances.

Details

Students are encouraged to take an iterative approach to porting and optimizing these industrial codes/kernels. The latter are of different nature/complexity and will allow the deployment of the classical phases of taking control of a scientific application. The evaluation of the teams (4 students maximum per team) will be based on the following points:

- **Porting**: it will be a question of validating the application on Arm architectures (Graviton2/Graviton3) by focusing on the test case provided by the industrial partner. The validation will be done by comparing the result files and/or by comparing the results on different platforms (x86/Arm).

- **Profiling**: Students will be asked to use classical application profiling tools to identify performance locks... this will include identifying the hotspots of these applications (compiler report, dynamic code analysis...)

- **Advanced optimization**: During this phase, the students will be able to make some modifications to the codes in order to improve the performances. For small applications (e.g., CGG code, this may involve adding OpenMP directives or modifying the organization of loops ...). In the case of complex code, participants can focus on the impact of the different compilation chains and work on extracting some kernels (mini-apps). The latter could then be the subject of specific efforts.

- Arm, Nvidia and GNU compilers will be available during the hackathon. Students will also have access to various code profiling tools.

- The synthesis of the obtained results (compilation recipes, validation procedure, optimization, loops extraction ...) will be made available on a Git repository in order to facilitate the evaluation and the reproducibility.

Proposed codes / Identified Kernels (September 2023)

CGG

Zeta of Riemann function: www.cgg.com

- Focus: numerical code optimization, from high-level algorithm to low-level optimizations (vectorization and code parallelism…). This reflects on real used-case from a scientific expert with a "non-optimized" and "non-parallelized" application looking to accelerate their code on a specific architecture. Quite a high capacity of transformation as long as the final result is correct.

EDF

Code Telemac: http://www.opentelemac.org/

- Focus: porting and numerical validation (intel/AMD comparison), evaluation of different compilers, possibly extraction of kernels (hotspots) for advanced analysis.

Format

Planning:

- Team registration: **Deadline on the 10th of November 2023**
- Webinar Presentation: **December 15th from 5:00 to 6:30 pm**
  - Presentation of the hackathon, the partners and the interest of the codes to be used + Q/A.
  - The webinar will be recorded and available all year
- Online dedicated session on training and the available tools: **beginning of January 2024**
- **Hackathon from Mond, 22nd of January 2024 at 9:00 am to Mond, 29th of January 2024 9:00 am.**
  - Estimated 48h work left to the choice of the institution within the week .
  - Team of 4 students
  - Available ARM/AWS support **from Mon, 22nd January 9:00 am to Frid, 26th of January 7:00 pm.**
- Prize Ceremony and feedback from students during the **Teratec Forum 2024: 30th of May 2024.**

Prize

The competition will result in a ranking, and the first team will be awarded a prize from ARM and CGG (4 MacBook Air), the second team will receive prizes offered by UCIT and EDF.

Donwload the presentation document about the Hackathon

Register to the 2024 Hackathon

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